Xgig BERT

Version 8.1

User's Guide

Xgig BERT

User's Guide

Viavi Solutions
1-844-GO-VIAVI
www.viavisolutions.com

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Contents

About this Guide

Congratulations on your purchase of the Xgig Maestro software which, depending on the licenses you obtain, includes Xgig BERT, Xgig Jammer, Xgig Generator, Xgig Target Emulator, Delay Emulator, and Xgig Load Tester.

Who Should Read this Guide

This guide is intended for networking professionals in research and development who need to monitor and test network performance. It is assumed that users of this guide have an engineering background.

What this Guide Contains

This guide is organized into seven chapters. The chapters contain the following information:

Chapter 1, “Introducing the Xgig BERT"” provides a description of the Xgig BERT features included since the last release Xgig Maestro.

Chapter 2, “Using the BERT Tab",” describes the Xgig BERT function tab interface and provides procedures to use it.

Chapter 3, “Configuring BERT Settings"” provides procedures and descriptions of the options for setting up a BERT pattern.

Chapter 4, “Configuring Latency Settings"” provides procedures and descriptions of the options for setting up latency measurements.

Chapter 5, “Using the Latency Tab"” provides procedures and descriptions of the options for running your latency measurement.

Chapter 6, “Bit Error Rate Testing on a Fibre Channel RAID *Application Note*"” describes how to use the Xgig BERT to test a Fibre Channel RAID.

Chapter 7, “Xgig BERT Troubleshooting Tips"” contains possible problems that you might encounter and provides solutions.

Appendix A, “Fibre Channel Ordered Sets - Partial List” contains some of the Ordered Set values that are used in this application.

Appendix B, “8-Bit/10-Bit Mapping” contains three tables: one is legal 8-bit/10-bit characters sorted by 10-bit value; the second is 10-bit values with no 8-bit mapping sorted by 10-bit value; the third is legal 10-bit values sorted by K/D code.

Appendix C, “Fibre Channel Legal Arbitrated Loop Physical Addresses” contains translation tables.

Appendix D, “Gigabit Ethernet Ordered Sets - Partial List” contains a table of these values.

Conventions

The following conventions are used in this guide.

Message Formats

This guide uses the following format to highlight special messages:

Note: This format is used to highlight information of importance or special interest.

Caution: This format is used to highlight information that will help you prevent equipment failure or loss of data.

Typographical Conventions

This guide uses the following typographical conventions:

bold sans serif	Commands
italics	Directory names, book titles, named key, for example the *Enter* key
courier font	Screen text, user-typed command-line entries

Technical Assistance

If you require technical assistance, call 1-844-GO-VIAVI (1-844-468-4284) or e-mail Techsupport-snt@viavisolutions.com.

For the latest TAC information, go to http://www.viavisolutions.com/en/services-and-support/support/technical-assistance.

Chapter 1

Introducing the Xgig BERT

In this chapter:

- Xgig BERT Features
- Xgig BERT Operation

This chapter describes the Xgig BERT (Bit Error Rate Tester) and how to use it to test gigabit serial devices.

The Xgig BERT allows you to:

- Test using bit error rate testing at 1.0625, 1.2500, 1.5000, 2.1250, 2.5000, 3.0000, 4.2500 and 8.5000 gigabit per second rates
- Verify physical layer components
- Send legal or illegal 8-bit and 10-bit patterns
- Measure latency

You can use Xgig BERT with Viavi test instruments; for example, it can be combined with the Xgig Analyzer to get more meaningful test results.

Xgig BERT Features

BERT is part of the Xgig Family of instruments. Xgig BERT has the following features:

- Up to 8.5000 gigabits per second (Gbps) Fibre Channel capability
- Xgig Maestro control window handles discovery and port set up for Xgig BERT
- Ability to control ports in a remote Xgig Chassis
- Ability to control multiple BERT ports at a time with one application
- Ability to share triggers with other devices in the same domain
- Improved status LEDs

  Three LEDs on the Xgig Maestro window provide status. Similar LEDs are also located on the front of the Xgig blades:

  — The Signal LED is a live indicator of Loss of Signal and Loss of Synchronization

  — The LOS LED provides latched information about Loss of Synchronization during a test

  — The Mismatches LED provides latched information about mismatches during a test
- Compare Zone can contain up to 4096 words
- Supports Fibre Channel Class 4 Ordered Sets
- Improved logging features

New Features

No new features have been released in this version of Xgig BERT.

Xgig BERT Operation

This section describes how patterns are transmitted to assist you in understanding how Xgig BERT operates.

If you want to create your own patterns to run, rather than use the patterns that are provided with the application, you use the BERT Configuration window.

Opening the BERT Configuration Window

If you want to create a configuration without assigning ports, on the main window menu bar go to:

File > New BERT Configuration > Bit error rate testing > Fibre Channel (Gigabit Ethernet)

To open this window with hardware assigned to the BERT:

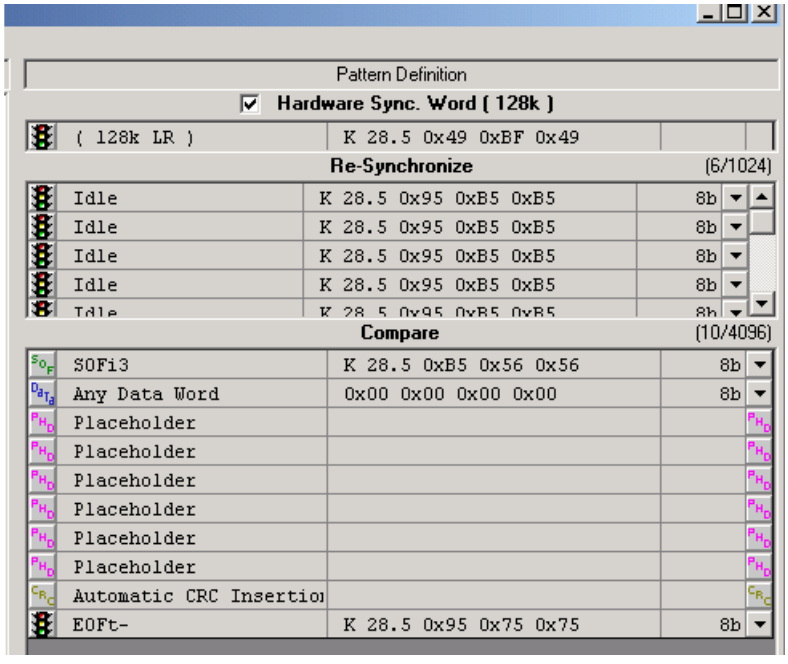
1. On the Port Selection and Domain Setup window, discover the chassis and use ports as BERTs. Refer to the *Maestro Introduction Guide* for details about how to do this.
2. Return to the Xgig Maestro main window and click on a device on the BERT tab.
3. Click the **Config** button.

   The BERT Configuration window is displayed. From this window you can create your own patterns. Refer to "Using the BERT Configuration Window" on page 46 for additional information about how to configure the BERT.

The Xgig BERT Pattern

When you look at the right side of the BERT Configuration window in its default form, you see the Pattern Definition window, divided into three sections (Figure 1). This is representative of what Xgig BERT sends.

Figure 1: Pattern Definition Window



When stopped, a user-definable word is sent repeatedly. You set this word in the **When stopped send**... box.

When you click **Start** on the BERT tab on the Xgig Maestro window, the following sequence occurs:

- Send 128k Hardware Sync Words to align the receiver (if enabled)
- Send the words in the Re-Synchronize (Re-Sync) Zone (if Re-Sync Mode is on)
- Send the words in the Compare Zone
- Loop from the bottom to the Re-Sync Zone again (or to the top of the Compare Zone if Re-sync Mode is off)
- Continue to loop until a stop condition is met.

Refer to "Pattern" on page 52 for more information about BERT patterns.

Patterns Sent and Received by Xgig BERT

Patterns are assembled and sent as 40-bit words. Often, those 40 bits represent four characters, symbols, or bytes as represented in 8-bit and 10-bit encoding. This device uses the Fibre Channel mapping of on-screen data to the wire. The data mapping is listed in Table 1.

Table 1: Fibre Channel On-Screen Data Mapping

Most Significant Character	Less Significant Character	Less Significant Character	Least Significant Character
Bits 76543210	7,6,5,4,3,2,1,0	7,6,5,4,3,2,1,0	1,0,1,1,1,1,0,0 K
Bits HGFEDCBA Z	H,G,F,E,D,C,B,A Z	H,G,F,E,D,C,B,A Z	H,G,F,E,D,C,B,A Z
8b to K/D Transform			
Z E D C B A H G F	Z E D C B A H G F	Z E D C B A H G F	K 1 1 1 0 0 1 0 1
K( ).( )	K( ).( )	K( ).( )	K(28).(5)
K/D to 10b Transform (Note that "a" is transmitted first)			
abcdeifghj	abcdeifghj	abcdeifghj	0 0 1 1 1 1 1 0 1 0

The least significant column in Table 1 shows an example of the 0xBC and a control flag converted into the well-known K28.5 "comma" character in a 10-bit space.

Most characters are data characters and can be represented in the form "Dx.y." There is a small set of characters called control characters that are represented as "Kx.y."

Note: Some blades give the option of enabling Fibre Channel Frame Scrambling, which is part of the Fibre Channel Specification for 8 Gbps. With scrambling enabled, all Fibre Channel BERT payload words are scrambled in 8-bit form and then encoded to 10-bit form, which means that the bits on the wire do not directly map to the 8-bit characters in the Configuration window.

8-Bit/10-Bit Encoding And Running Disparity

The 8-bit/10-bit encoding method is used to maintain DC balance in the cable by having nearly equal 1s and 0s, as well as having a transition-rich environment for maintaining a clock recovery phase locked loop. Only 10-bit characters that have 4, 5, or 6 ones present are legally used. In general, if a character has 6 ones the next non- 5 ones and 5 zeros character will have 4 ones. Most bytes have two possible 10-bit encodes whose usage depends on the running disparity left by the previous symbol. Refer to Appendix B, "8-Bit/10-Bit Mapping" for a list of 8-bit/10-bit characters.

Running disparity for a transmission character is calculated on the basis of sub-blocks, where the first 6 bits (abcdei) form one sub-block (6-bit sub-block) and the second 4 bits (fghj) form the other sub-block (4-bit sub-block). The running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the last transmission character. The running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the transmission character is the running disparity at the end of the 4-bit sub-block. Running disparity for the sub-blocks is calculated as follows:

- Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
- Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
- Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Note: All sub-blocks with equal numbers of zeros and ones are disparity neutral. In order to limit the run length of 0s or 1s between sub-blocks, the 8-bit /10-bit transmission code rules specify that sub-blocks encoded as 000111 or 0011 are generated only when the running disparity at the beginning of the sub-block is positive. Running disparity at the end of these sub-blocks is also positive. Likewise, sub-blocks containing 111000 or 1100 are generated only when the running disparity at the beginning of the sub-block is negative. Running disparity at the end of these sub-blocks is also negative.

Fibre Channel Ordered Sets

Fibre Channel utilizes special words beginning with K28.5 followed by three bytes. These are called Ordered Sets. Refer to Appendix A, "Fibre Channel Ordered Sets - Partial List."

Legal (Neutral Disparity) Arbitrated Loop Physical Addresses

Fibre Channel has a separate specification for Arbitrated Loop. This specification allows up to 126 devices to be placed in a loop and communicate directly with each other. These devices have disparity-neutral addresses rather than the three byte addresses normally used by switched networks. Not all characters can be used as a Loop ID value. There is a specific list of characters that are disparity-neutral. Some of these characters are mapped the same regardless of running disparity, while others are inverted (ones complement). Refer to Appendix C, "Fibre Channel Legal Arbitrated Loop Physical Addresses" for this information.

Gigabit Ethernet Ordered Sets

Gigabit Ethernet utilizes special characters called Ordered Sets that usually consist of at least one control character. These include I1 (K28.5 0xC5), I2 (K28.5 0x50), R (K23.7), S (K27.7), T (K29.7), and V (K30.7). Refer to Appendix D, “Gigabit Ethernet Ordered Sets - Partial List.”

Receiver Limitations

While the transmitter can send almost anything, there are some bit pattern requirements and limitations for the Xgig BERT receiver. The Xgig BERT receiver recovers the clock from the incoming 10-bit pattern using a phase locked loop (PLL). This places the following list of requirements on the incoming signal:

- Have a received clock rate within 250 ppm of the Xgig BERT transmit clock rate. The receiver switches over to its internal transmit clock if the received signal is too fast or too slow.
- Use legal 10-bit values and disparity rules whenever possible.
- Avoid runs of seven or more consecutive 1s or 0s.
- Have at least 3 transitions between 1 and 0 in a 10-bit character for the PLL to maintain tracking.
- Maintain DC balance by having 20 +/- 1 (that is, nearly the same number) of 1s and 0s in a 40 bit word, wherever possible.
- Transmit K28.5 (commas) only in allowed position(s) within the word, depending on the protocol.
  - — In Re-Sync mode (described later), you must use negative starting disparity K28.5 (0011111010) symbols for character and word alignment. Never transmit the pattern 0011111 in an unaligned position (in the wrong byte or across bytes or words). This is the comma indicator and the re-synchronizing hardware will bit shift the received pattern to put those seven bits in the expected aligned position (depending on protocol).
  - — When re-synchronization is not enabled, the Xgig BERT can receive comma characters in any byte position.
- Use a known, good cable and/or loopback adapter to validate that the pattern can be received without errors before testing an unknown device.

Chapter 2

Using the BERT Tab

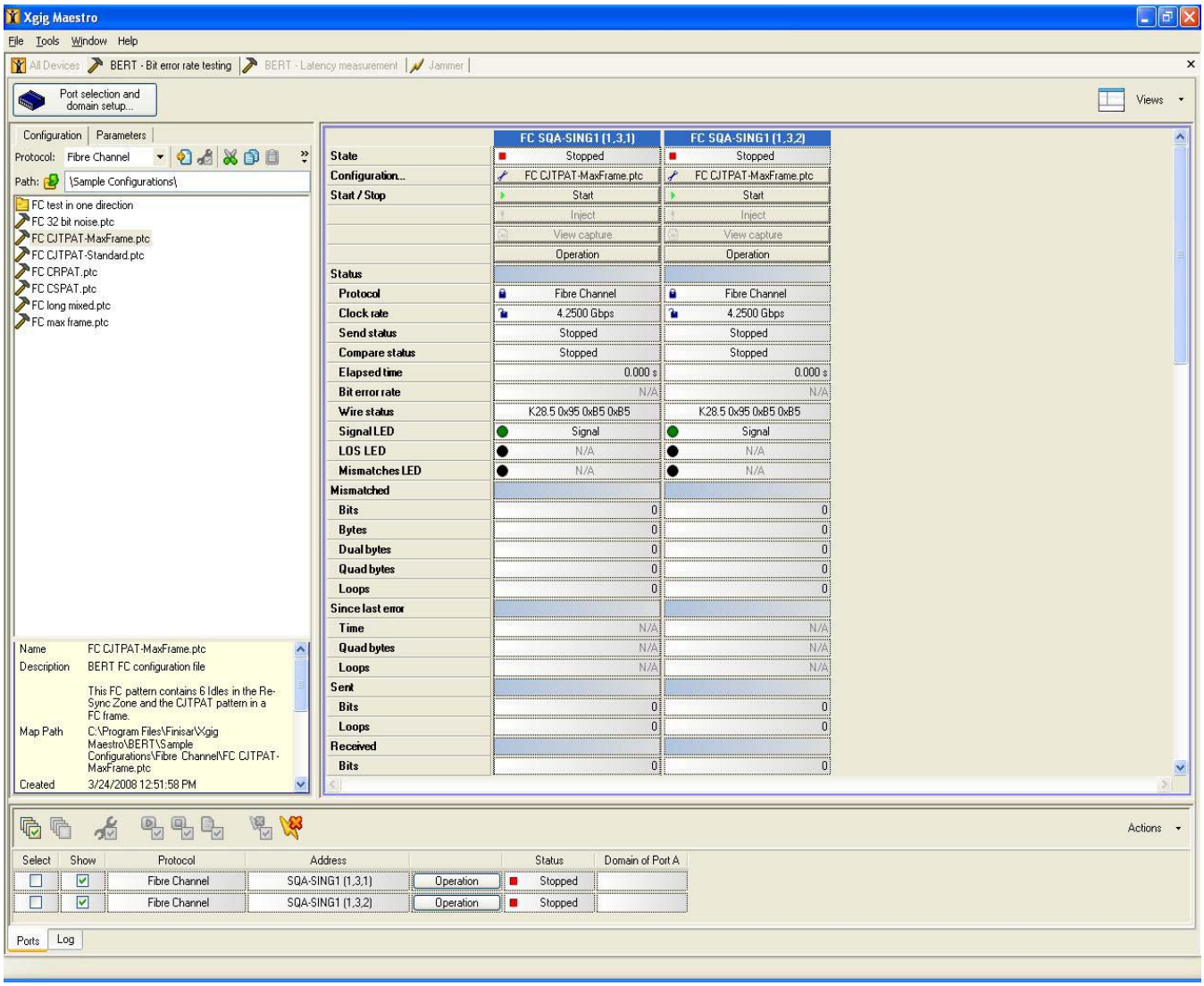
In this chapter:

- Using the Configuration Manager in BERT
- Using the Parameters Status Table in BERT
- Using the Parameters Status Context Menu in BERT
- Using the Ports Manager in BERT
- Using the Log Manager in BERT
- Using the Capture Commands
- Customizing the Appearance of the Maestro/BERT Main Window
- Performing Configuration Tasks in BERT
- Running a BERT Pattern

After you have discovered and locked the BERT ports you want to use and also set up your capturing and monitoring applications, such as Xgig Analyzer, you are ready to run the Xgig BERT application. This chapter provides an overview of the BERT tab and its functions; it also includes steps to run predefined tests supplied with Xgig BERT or tests you have defined and saved.

You should have launched Xgig Maestro as described on in the *Maestro Introduction Guide* and locked at least one device. The Xgig Maestro window (Figure 2) is displayed with the BERT tab on the right. This tab is where you operate the BERTs you have locked.

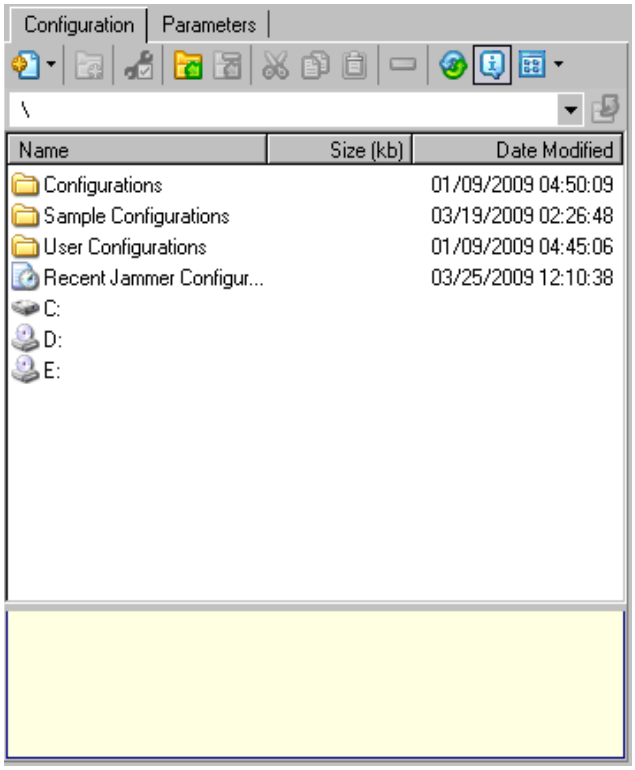
Figure 2: Xgig BERT Tab on the Xgig Maestro Window



Using the Configuration Manager in BERT

The Configuration manager (Figure 3) is associated with the device function tab, BERT and Jammer. The configuration files displayed in the manager are specific to the function tab displayed. The Configuration manager provides a list of test configurations organized in three folders. The **Sample Configurations** folder includes configurations that are provided with the application. The **User Configurations** folder is where the configurations you create are saved. The **Most Recently Used** folder allows you easy access to those configuration files most recently used.

Figure 3: BERT Configuration Manager



The Configuration manager has the following features:

- Protocol selection menu

  The drop-down menu lets you select the protocol for the device you are using:

  — Fibre Channel

  — Gigabit Ethernet

- Folder with a list of sample test configurations by device and protocol
- Folder for configurations that you created by device and protocol
- Tool bar that lets you create, load, copy, cut, and paste configuration files. See “Configuration Manager Tool Bar in BERT” on page 12 for more information on this tool bar.

- Context menu

  Select a configuration file name and right-click to display a menu where you can choose to create and edit configuration files, and additional operations. See “Configuration Manager Context Menu in BERT” on page 13 for more information about these menus.

- Drag and drop files

  You can drag any configuration from the Configuration manager list onto a device column to load it.

- Browse to map folders of files stored in locations other than the default Sample and User Configuration folders.

- Description pane

  — When you select a configuration file in the list, a description of the file is displayed in the description pane below. It also displays the name of the file, the path where the file is located, the size of the file, the date and time when the file was created, the date and time the file was modified, whether the file is read-only and the Map path where the file is located on your system.

  — When you click the Show/Hide button below the Description pane, you display or hide this pane.

- Recently-Used

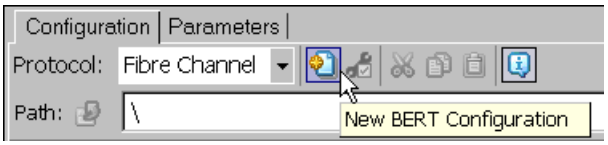
  — You can access recently-used BERT files.

Configuration Manager Tool Bar in BERT

The Configuration manager tool bar (Figure 4) allows you to perform the following functions:

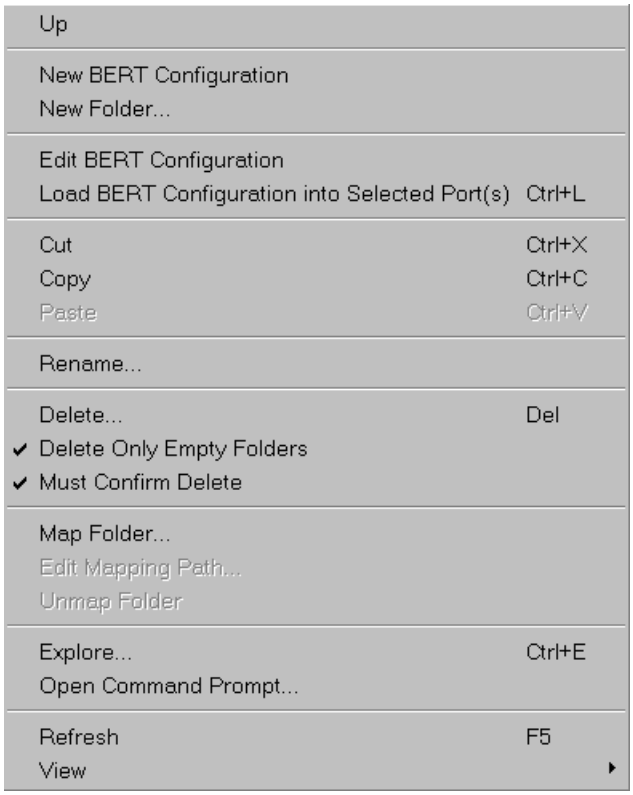
Click the **New Configuration** icon to open the Configuration window and create a new BERT configuration from scratch. You can also highlight a file and use the **Cut**, **Copy**, and **Paste** icons to duplicate or move files in the Configuration manager into another folder using the **Path** shortcut. The Load icon allows you to load a configuration file into a port or ports. This icon is only active when a port has been locked and is selected in the Port Manager. See “Loading BERT Configuration Files” for details.

Figure 4: BERT Configuration Manager Tool Bar



Configuration Manager Context Menu in BERT

Figure 5: Configuration Manager Context Menu in BERT



Right-click in the list to choose the following actions from the context-sensitive menu:

- **Up**

  Displays the contents one folder level up from the current display.

- **New BERT Configuration**

  Opens a new BERT configuration window for editing.

- **New Folder**

  Opens the Configuration manager dialog where you can enter the name of a new folder you want to add.

- **Edit BERT Configuration**

  Opens the file highlighted in the list, the same as double-clicking on the file name.

- **Load BERT Configuration into Selected Port(s)**

  Loads the file highlighted in the list into the port(s) selected in the Ports Manager. See “Using the Ports Manager in BERT.”

- **Cut**

  Removes a selected file or folder from the list.

- **Copy**

  Copies a selected file or folder to a clipboard making it available to paste in another location.

- **Paste**

  Pastes a file or folder you cut or copied to the location you choose.

- **Rename**

  Opens a dialog with the current file or folder name displayed in an entry field that you can modify. It also shows the protocol, path, and current file or folder name.

- **Delete**

  Opens a dialog where you can confirm whether you want to delete the highlighted file (configuration) or folder from the list.

- **Delete Only Empty Folders**

  Sets this choice as a preference that removes only empty folders from the list. When you select it, a check mark is displayed next to it. It is selected by default.

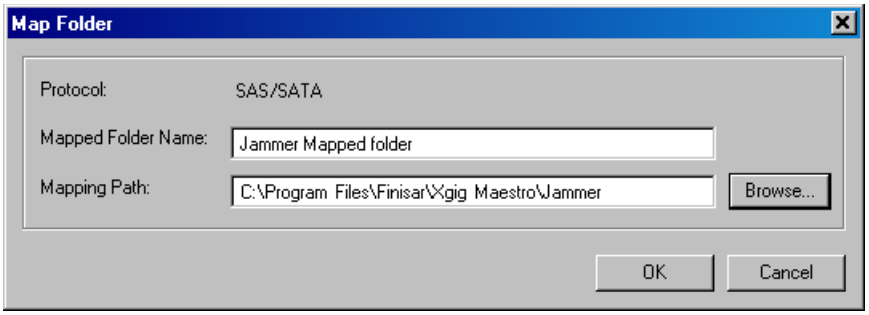
- **Must Confirm Delete**

  Sets this choice as a preference that opens a dialog to confirm that you want to delete a file or folder from the list. When you select it, a check mark is displayed next to it. It is selected by default.

- **Map Folder**

  Opens the Map Folder dialog box that lets you map a folder to a name of your choice.

Figure 6: Map Folder dialog box



Enter a name of your choice in the Mapped Folder Name field, and use the **Browse** button to select the folder on your system or network you want to map to this name.

- **Edit Mapping Path**

  Allows you to edit the mapping path.

- **Unmap Folder**

  Removes a highlighted mapped folder from the Configuration manager.

- **Explore**

  Opens a Windows Explorer window showing the directory where the current configuration files are located.

- **Open Command Prompt**

  Opens a Windows Command Prompt window showing the directory where the current configuration files are located.

- **Refresh**

Refreshes the Configuration Manager window.

- **View**

  Has two choices:

  — List

  Displays the list of files or folders in the path you choose.

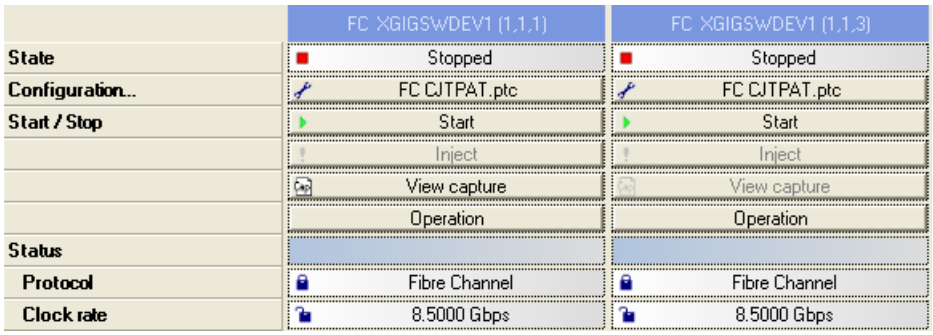
  — Details

  Displays the list of files or folders with the size and modification date.

Using the Parameters Status Table in BERT

Each BERT device is displayed as a column in the Parameters Status table on the BERT tab (Figure 2). At the top of each column is the protocol, chassis name, followed by the chassis number, the slot number and port number in parentheses. (Figure 7).

Figure 7: BERT device displayed as a column in the Parameters Status table



Each column contains the following categories:

- State
- Configuration
- Start/Stop
- Status
- Sent
- Received
- Compared
- Mismatched
- Since last error

State Category

This category shows the BERT status: Disconnected, Connecting, Starting, Synchronizing, Running, Stopping, Stopped.

Configuration Category

Displays the name of the configuration, if any, loaded into the port. Refer to “Loading BERT Configuration Files” on page 42.

You can press the button bearing the name of the loaded configuration file to open the Configuration Edit window.

Start/Stop

This category contains the buttons to operate each BERT device.

Start/Stop

Start runs a test pattern from the beginning if you click it while the BERT is stopped. When you click **Start**, the Mismatched LEDs and LOS status LEDs are cleared on the Parameters Status table.

Stop causes the BERT to abort running the test pattern and end the test. The BERT always stops sending after it finishes the loop it is sending, and stops comparing after it finishes the loop it is comparing.

Inject

Inserts a bit error while a test is running. The bit error is placed only among words in the Compare Zone of the defined pattern (except the Start Word). In the 40 bit word, bit 19 or 18 is inverted to create the bit error.

View capture

Downloads and displays the captured data of the test you have performed.

Operation

Opens the Operation dialog box

Status Category

This category indicates the current physical setup of the BERT device.

Protocol

Indicates the protocol of the BERT, either Fibre Channel or Gigabit Ethernet. You choose a protocol in the Port Selection and Domain Setup window when you lock ports. The small lock icon indicates that the protocol cannot be changed at this stage.

Clock rate

Indicates the BERT clock rate. It cannot be changed while the BERT is running. The closed lock icon indicates you cannot currently change the clock rate; the open lock icon indicates you can change the clock rate. The clock rate options may include 1.0625 Gbps, 1.2500 Gbps, 2.1250 Gbps, 2.5000 Gbps, 4.2500 Gbps, or 8.5000 Gbps, depending on the blade. Both ports in a port pair must always be set to the same clock rate. Therefore, if you have two BERTs, and one of them is running, the clock rate is locked on both of them.

Domain of Port

Displays the domain name to which a port belongs, if any.

Send Status

The Send Status metric reflects the state of transmitting hardware and reports:

- Stopped
- Waiting for trigger input
- Sending hardware sync
- Sending...
- Stopping...

Compare Status

The Compare Status metric reflects the state of the compare hardware and reports:

- Stopped
- Trying to sync up
- In hardware sync
- Receiving...
- Waiting for trigger input
- Stopping...

Elapsed time

The Elapsed time metric is the period of time since you started the BERT operation and it runs until the BERT is stopped.

Bit error rate

The Bit Error Rate metric is a computed value. When no errors have occurred, the formula is:

```
< 1/(Bits Compared)
```

After an error occurs, the formula changes to:

```
= (Bits Mismatched)/(Bits Compared)
```

Wire status

Shows the current output of the port.

Signal LED

This LED always shows what is occurring at that moment in a test and therefore changes instantaneously. Table 2 describes the LED colors.

Table 2: Signal LED Descriptions

Port column LED color	Blade LED	Description
Green	Green	Signal is detected and the link is synchronized.
Red	Yellow	Loss of synchronization is occurring.
Black	Off	No signal detected on the link.

LOS LED

The loss of synchronization (LOS) LED shows if loss of synchronization has occurred during the current test (if running) or during the previous test (if stopped). The LED is reset when you start the BERT. The LED colors are described in Table 3.

Table 3: LOS LED Descriptions

Port column LED color	Blade LED	Description
Green	Green	The link is synchronized.
Yellow	Yellow	Loss of synchronization was detected at some point while the test was running.
Red	Blinking Yellow	Loss of synchronization is occurring now or in the last 5 seconds.
Black	Off	Not applicable.

Mismatches LED

The Mismatches LED shows if mismatches have occurred during the current test (if running) or during the previous test (if stopped). The LED is reset when you start the BERT. The LED colors are described in Table 4.

Table 4: Mismatches LED Descriptions

Port column LED color	Blade LED	Description
Green	Green	No mismatches occurred during the test.
Red	Blinking Yellow	A mismatch occurred in the last 5 seconds.
Yellow	Yellow	Mismatches were detected.
Black	Off	Not applicable.

Log

This item is hidden by default. **Log available** displays if a log from the last operation is available for viewing. You can view the log, save it to a file, and set up automatic naming and file saving from the Log menu in the Parameters context menu. To use these menu items, refer to "Using the Log Manager in BERT" on page 29.

Capture

This item is hidden by default. **Capture available** displays if a capture from the last operation is available for viewing. You can view the capture log, save it to a file, and set up automatic naming and file saving from the Capture menu in the Parameters context menu. To use these menu items, refer to "Using the Capture Commands" on page 35.

Sent, Received, Compared, Mismatched Categories

Table 5 summarizes these metrics in the Parameters Status table and lists the criteria that the BERT uses to check for errors.

Table 5: Transmitter and Receiver Metric Error Checking

	Bits (40/Word)	Bytes	Dual Bytes	Quad Bytes	Loops
Sent	QB * 40	QB * 4	QB * 2	Counted	Counted
Received	QB * 40	QB * 4	QB * 2	Counted	Copy of compared
Compared	QB * 40	QB * 4	QB * 2	Counted	Counted
Mismatched	Counted	Counted	Counted	Counted	Counted
Since Last Error				Counted	Counted

The following list describes the data in the Parameters Status table that the BERT offers as statistics:

- Bits: Computed values, quad bytes (QB) x 40 bits/quad byte, except Mismatches are counted per bit.
- Bytes: Computed values, QB x 4, except Mismatched counts bytes with 1 or more errors.
- Dual Bytes: Computed values, QB x 2, except Mismatched counts byte pairs with 1 or more errors. Byte pairs are bytes 0 and 1, and bytes 2 and 3.
- Quad Bytes: Counted values, Mismatched counts words with 1 or more errors as only 1 word.
- Loops: Counted values, except Received Loops equals Compared Loops

Notice that the compare state machine waits for the first compare word to be matched before beginning. If the transmitted pattern is corrupted, the first word might not be found. If the first word is not found, no loops are compared. Under this circumstance the number of Received Bits count rapidly but, Compared Bits, Bytes, Dual Bytes, Quad Bytes and Loops are not incremented.

Since Last Error Category

Time

The Time since last error metric is the elapsed time since the last mismatch was observed.

Quad bytes

The number of quad bytes received since the last mismatch occurred. Is not available when loss of sync disrupts the counting of bits.

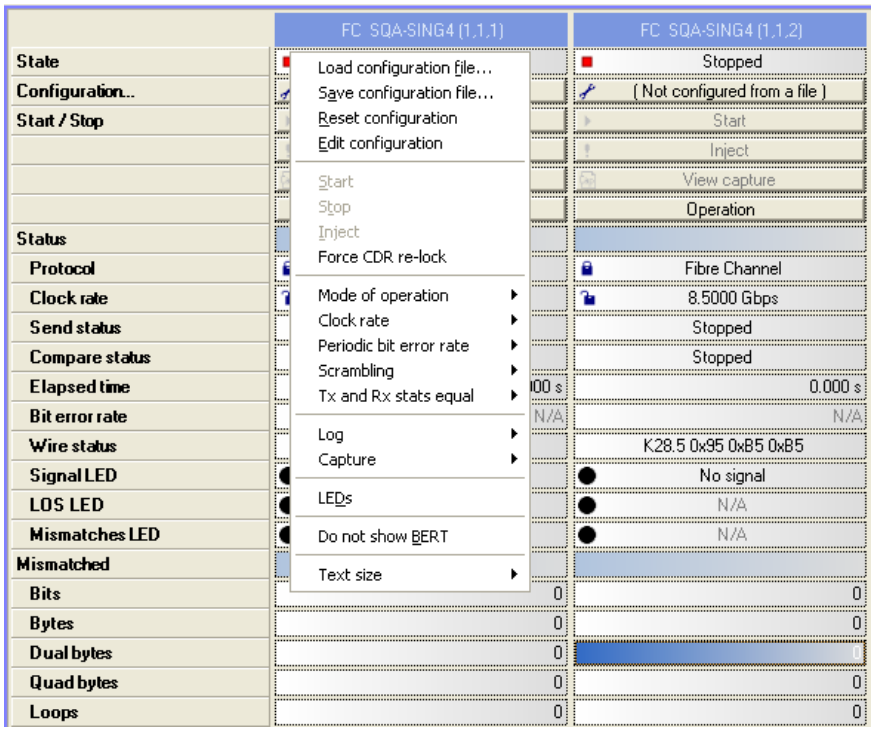
Loops

The number of loops received since the last mismatch occurred. Is not available when loss of sync disrupts the counting of bits.

Using the Parameters Status Context Menu in BERT

Right-click on a Parameters status column to display the context menu. The available operations are displayed for the column in which you click. This menu provides controls for configuration files, operation, setting clock rates, setting BERT or Latency mode of operation, choosing capture options, logging test activity, removing a BERT from the Parameters Status table, and changing the appearance of the status table.

Figure 8: BERT Parameters Context Menu



Changing the Clock Rate in BERT

To change the clock rate:

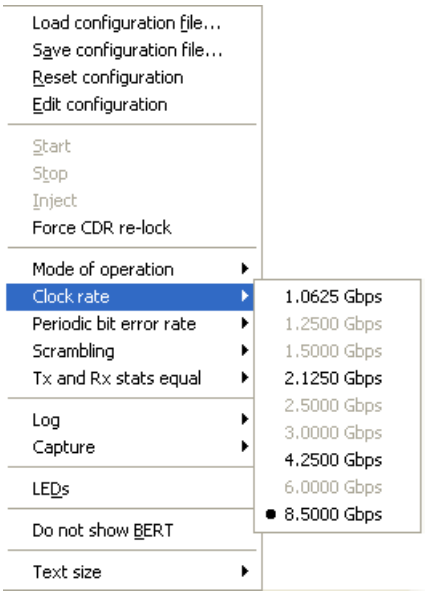
1. Right-click anywhere on the specific port column to open the Parameters context menu (Figure 9).
2. Select **Clock rate**.

   A menu with available choices is displayed.
3. Click to choose one.

   Items that are grayed out are not currently available. A bullet is displayed to the left of the currently operating selection.

Note: The clock rate is not saved in the configuration file. This allows BERT configurations to run independently of the clock rate setting and avoids disrupting the traffic where the BERT is connected.

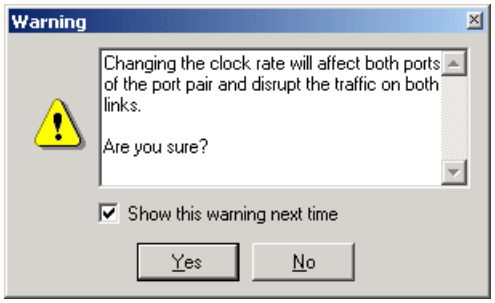
Figure 9: Clock Rate Menu



Note: BERT ports 1 and 2 always share the same clock rate; the same is true of ports 3 and 4 (on a four port blade).

Note: Changing the clock rate disrupts the traffic sent by the BERT. A warning message appears when you change the setting (Figure 10).

Figure 10: Changing Clock Rate Warning



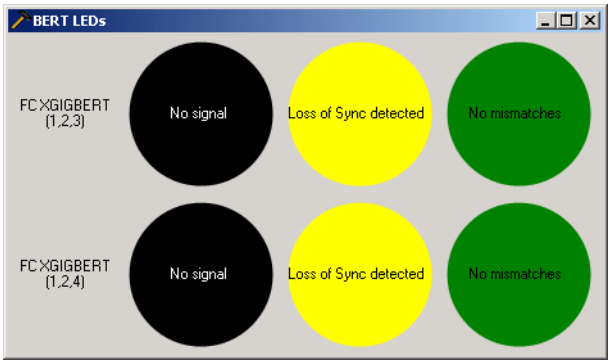
Viewing Port LEDs

LED icons are displayed next to Signal LED, LOS LED and Mismatches LED in the Parameters Status table. To view these LEDs in a larger format:

>> Select LEDs from the Parameters context menu.

The LEDs for the ports you have locked are displayed in a dialog (Figure 11).

Figure 11: BERT LEDs Dialog



Scrambling

Some blades give the option of enabling Fibre Channel Frame Scrambling, which is part of the Fibre Channel Specification for 8.5000 Gbps. You may enable or disable scrambling at any speed. Select **Scrambling** from the Parameters context menu, and then select **Enabled** or **Disabled**. A check mark appears next to the current selection. When Scrambling is enabled, Fibre Channel Frame Scrambling is performed in the Configuration pattern starting after any SOF indicator template and continuing until the next word with a K character (usually EOF).

Note: When changing the clock rate from 8.5000 Gbps to any other speed, Scrambling is automatically set to Disabled. When changing to 8.5000 Gbps, it is automatically set to Enabled. You may then override this setting using the Parameters context menu.

Tx and Rx Stats Equal

When this feature is enabled, the Send and Receive statistics are forced to be equal in each run.

When a run is started, the words in the Re-Sync Zone of the initial loop prior to the first Compare Zone are not counted in the statistics on the sending side. Similarly, the words before the first Start Word are not counted in the statistics on the receiving side.

When a run is stopped, the sending side sends an additional CLS Ordered Set. The receiving side waits for this additional CLS Ordered Set before stopping. A timeout is implemented in case the last CLS Ordered Set is never received.

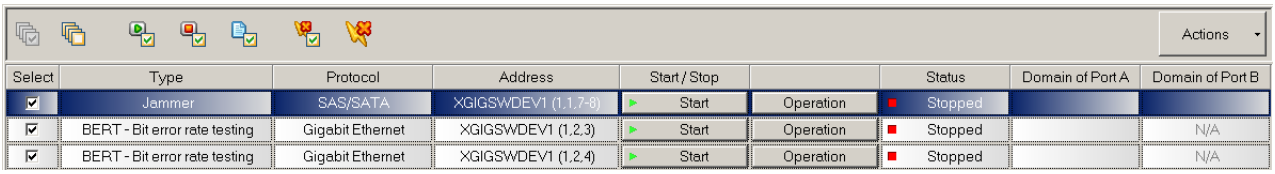
Note: The Tx and Rx Stats Equal option is only available on the 8.5000 Gbps Fibre Channel blade.

Using the Ports Manager in BERT

The Ports manager displays details about the ports you have locked. It shows the protocol, chassis name (with chassis number, slot number, and port numbers), and other port specific information. You can sort the rows from first to last or last to first by clicking the column heading. For more information about Xgig slot positions and numbering, refer to the Xgig Family Hardware Guide included with the product CD.

Note: If you are disconnected due to a network problem, you can reconnect to the ports by using the Port Selection and Domain Setup window.

Figure 12: BERT Ports Manager



The following icons are displayed on the menu bar:

Select All Ports
Selects all ports in the Ports Manager.

Unselect All Ports
Unselect all ports in the Ports Manager.

Load Configuration to Selected Ports
Load the selected configuration file to all selected ports in the Ports Manager.

Start Selected Ports
Start BERT operation on the selected ports in the Ports Manager.

Stop Selected Ports
Stop BERT operation on the selected ports in the Ports Manager.

Show Properties of Selected Ports
Display the Port Properties dialog box, with information on the selected function, protocol, and clock rate (speed). It also shows the chassis name, IP address, slot and port(s).

Disconnect Selected Ports
Disconnect the selected ports in the Ports Manager.

Disconnect All Ports
Disconnect all ports in the Ports Manager.

Actions Button

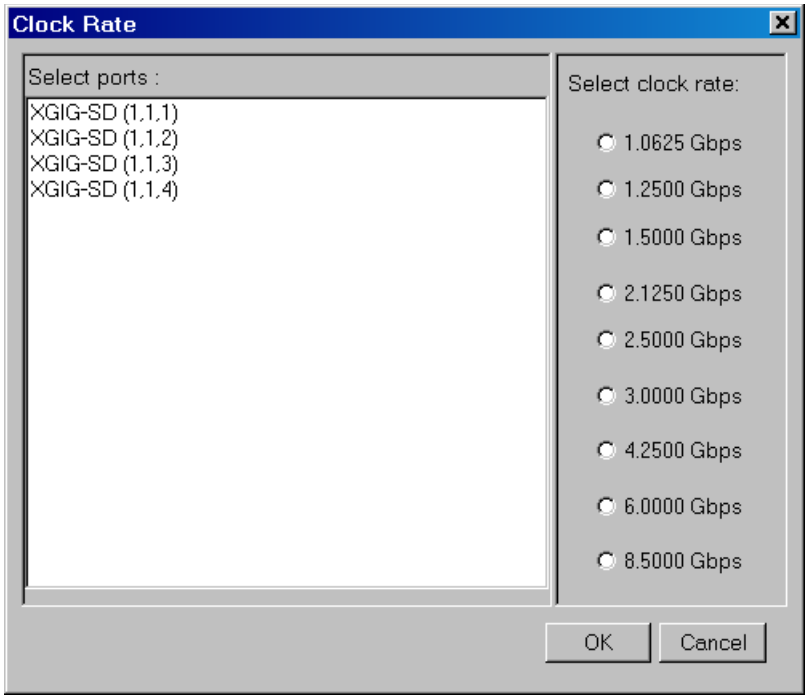
The **Actions** button contains menus for **Multiple speed Change** and **Toggle Display**. See Figure 13.

Figure 13: Actions Button Options

Multiple Speed Change

This option allows you to change the speed of multiple BERT ports simultaneously. If you have the All Devices tab selected, the menu will display BERT, Jammer, and Generator.

Figure 14: BERT Multiple Speed Change Window



Select the ports you want to change the speed for, holding the Ctrl key down to select multiple ports, then click the speed you want to change to, and click **OK** to apply the change.

Toggle Display

This option toggles between a horizontal and vertical view of the ports.

Ports Manager Columns

The Ports Manager includes the following columns:

Operation

Operation is a button you press to display the Operation bar for the device you are using. Refer to “Running a BERT Pattern” on page 44 for additional information.

Status

Information in this column displays the state of the device under test.

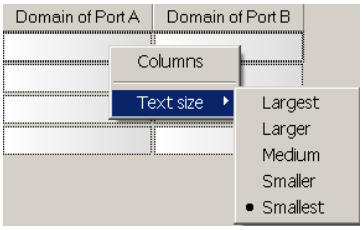
Domain of Port A and Domain of Port B (BERT and Jammer only)

Each of these fields indicates to which domain the respective port belongs. In a simplex Jammer, only port A is relevant. In a duplex Jammer, the lower port number is always port A. You set up domains in the Port Selection and Domain Setup window. Refer to the “Using Domains” section of the *Maestro Introduction Guide* for more information.

Using the Ports Manager Context Menu

You can right-click in the Ports Manager to open the context menu (Figure 15).

Figure 15: Ports Manager Context Menu



The menu contains the following choices:

Text Size

Refer to “Changing Text Size” on page 39 for information.

Columns

This choice opens a Customize table dialog (Figure 16) where you can choose to display **Domain of Port A**.

Click the check box next to this item to display this item in the Ports Manager.

The grayed out items are defaults; you cannot clear these items.

Figure 16: BERT Ports Manager Context Menu Parameters Selection

Using the Log Manager in BERT

To access the Log Manager, click the Log tab at the bottom of the BERT main window.

The purpose of logging is to automatically create a log that reports the results of a BERT test. You can view a log with any text editor.

Note: The log buffer can be up to 10000 entries. During a single test run, if more entries are collected than the maximum number you specified, only the most recent 10000 are logged. You set the maximum number of entries in the Log Options window.

The Filter icons next to the **Type** and **Address** column labels allow you to choose how you want to display device types, by protocol or All, and device addresses, by single address or All devices.

If the **All Devices** tab at the top of the Xgig Maestro main window is selected, then the **Log Source** menu 

shows all log sources as active by default. You can choose to disable BERT logging, Jammer logging, Generator logging, Target Emulator or all four by clicking the **Log Sources** menu and un-checking the selections. If the **BERT-Bit error rate testing, Jammer, or Generator** tabs in the main window are selected, then the Log Manager displays only the log entries for that tab, respectively.

The following icons are displayed on the Log Manager menu bar:

Display Entry Contents
Lets you save the selected log to a file in the device (BERT or Jammer) Logs folder (for example: C:\Program Files > Viavi > Xgig Maestro > BERT> Logs) or anywhere you want to save it on the network.

Save All Entries As
Lets you save all the logs in the Log Manager to a file.

Save selected entries as
Lets you save the selected logs to a file.

Select All
Selects all the logs in the Log Manager.

Options
Opens the Log Manager Options dialog where you can enter your preferences for the information you want displayed in the Log Manager (Figure 17).

Clear Filtering
Removes filtering by Type and Address and displays all the devices you have locked.

Clear Selected Entries
Deletes the log entry you have highlighted.

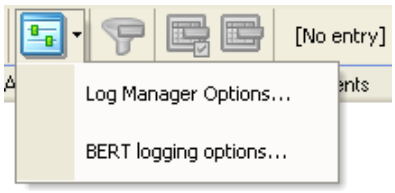
Clear All Entries
Deletes all the log entries in the Log Manager.

Setting Log Options

To have log files automatically named and saved to a specific location:

1 Click the Log Manager Options icon to open the drop-down menu (Figure 17) and select **BERT logging options**.

Figure 17: Log Manager Options Menu



Or:

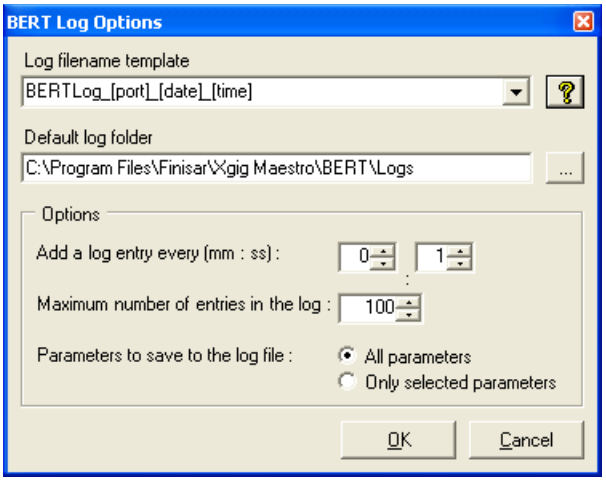
>> Open the Parameters context menu (Figure 22) and select **Options**.

This command opens the BERT Log Options dialog (Figure 18). It allows you to set up how you want the log files to be automatically named and where you want them saved by default.

The Options area of the dialog lets you:

- Enter the number of minutes and seconds for each log entry to be added
- Enter the maximum number of entries you want in a log
- Select the parameters to be saved to the log file — all parameters or the parameters you chose to display on the Parameters Status table in the Customize table dialog.

Figure 18: Log Options Dialog



2 Select a log filename template from the following choices:

- BERTLog_[port]
- BERTLog_[port]_[date]_[time]
- BERTLog_[date]_[time]
- BERTLog_[date]_[time]_[port]

Or, you can type in your own template. The port, date, and time markers are replaced with their corresponding values. Port is displayed as:

```
protocol (FC or GE), chassis name (chassis number in the cascade,
blade number in the chassis, port number on the blade)
```

3 To set specific time intervals for statistics to be polled, enter minutes and seconds in the Add a log entry every (mm : ss) field.

4 To set the number of entries in a log, enter the number.

The default is 100. The minimum number of entries is 1 and the maximum number of entries is 10,000. When a log reaches the maximum number of entries, it drops the oldest entry each time a new one is added.

5 To save specific parameters you have chosen in the Parameters Customize Table dialog, click the Only selected parameters radio button.

The default is to save all the parameters to the log.

6 Enter the path to the folder where you want to save the log file.

You can browse to where you want to save the log file by clicking ... .

7 Click **OK**.

You have set up the log filename template and default folder to save the log.

Note: Log options are the same for all BERT ports.

Viewing a Log

The Xgig BERT log lists a periodic snapshot of all the statistics you choose (Figure 21). The time between snapshots and the statistics that are logged are two settings available in the Parameters context menu.

To display a log:

>> Click the Log Manager tab at the bottom of the Xgig Maestro main window to view the log in a tabulated format (Figure 19).

Or you can:

>> Double-click on the log you want to view in the Log Manager and display the Log Entry Display window (Figure 20).

Or:

>> Click the **Operation** button for the device in either the Parameters Status table or the Ports manager to open the Operation dialog bar. Then click the **Log** icon.

Or:

>> Open the Parameters context menu and select **Log > View**

The two latter commands open a window (Figure 21) that allows you to quickly view the Xgig BERT log. Click **Print** at the bottom of the BERT Log to print a hard copy of the log. In the case of these two methods, each time you run a BERT pattern, a new BERT Log is created for that device, and the previous log is discarded.

On the other hand, the Log Manager continues to list the logs and display them depending on the Log Manager options you have selected. See “Setting Log Options” on page 30.

You can save a log to a `.txt` file or an HTML file. Refer to “Saving a Log” on page 33.

Figure 19: Log Manager

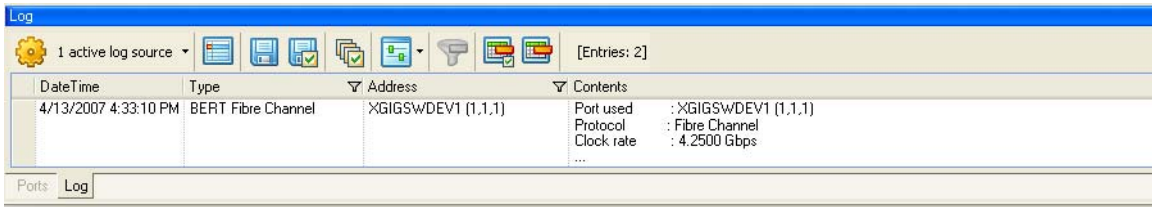


Figure 20: Log Entry Display Window

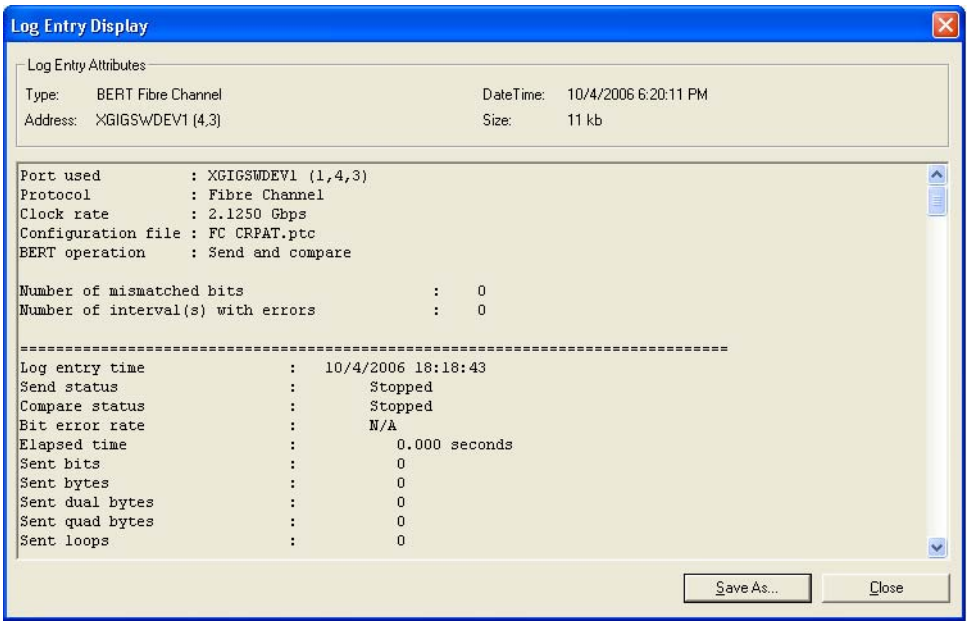
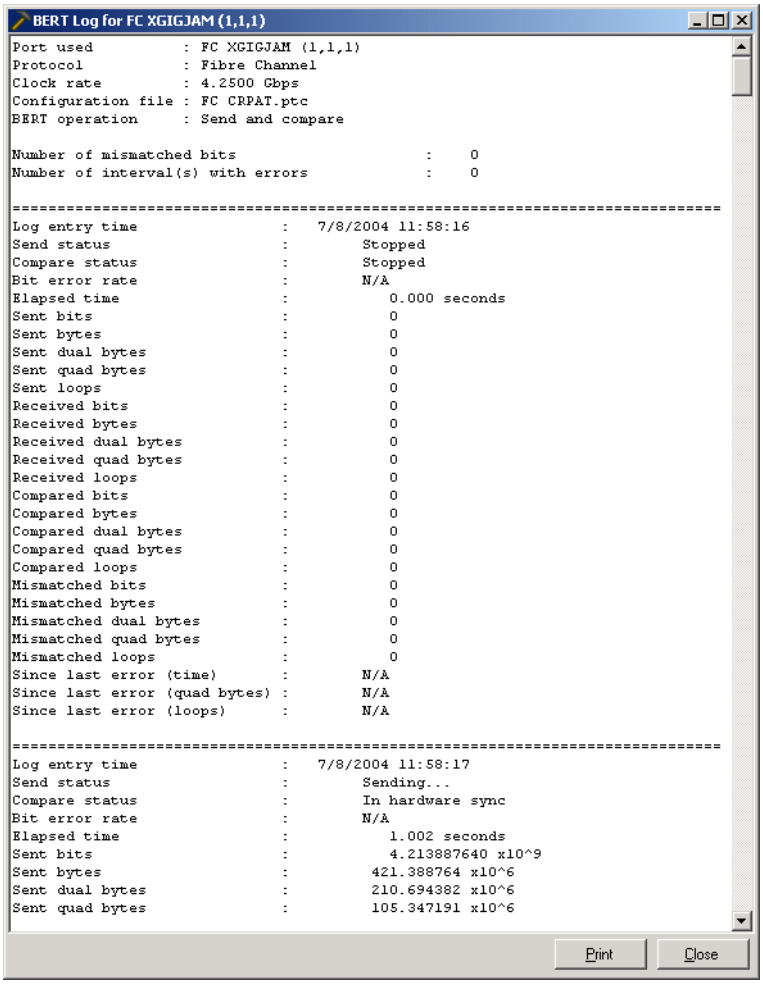


Figure 21: Example of a BERT Log



Saving a Log

You can save a log to a `.txt` file or an HTML file. You can use the Log Manager tab or the Parameters context menu to accomplish this.

To save a log from the Log Manager tab as an HTML file or a text file:

1 Highlight the log you want to save.

2 Click the **Save Selected Entries As...** button.

The Save Log Manager Contents As window is displayed that lets you name and save the log as an HTML file to the Saved Logs folder or to a location you prefer.

Or:

Double-click on the log you want to save to display it in the Log Entry Display window (Figure 20), then click **Save As...**

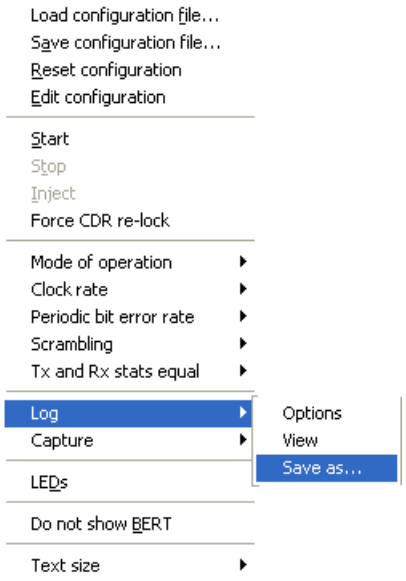
The Save As window is displayed that lets you name and save the log to the Logs folder as a `.txt` file, or to a location you prefer.

To save a log to a `.txt` file using the Parameters context menu:

>> Open the Parameters context menu (Figure 22) and select **Log > Save As**.

This command opens a File dialog where you can save the log with a file name you assign to it.

Figure 22: Log Menu



Using the Capture Commands

You can view, save, and set saving options by using the BERT capture commands. These commands are available in the Operation bar and the Parameters context menu.

Viewing a Capture

You can display a window that allows you to quickly view the Xgig BERT capture file. The capture shows 4096, 40-bit words in 10b format (Figure 21). You can print the capture log from this window.

To display a capture log:

>> Click the **View Capture** button of the specific BERT in the Parameters Status table.

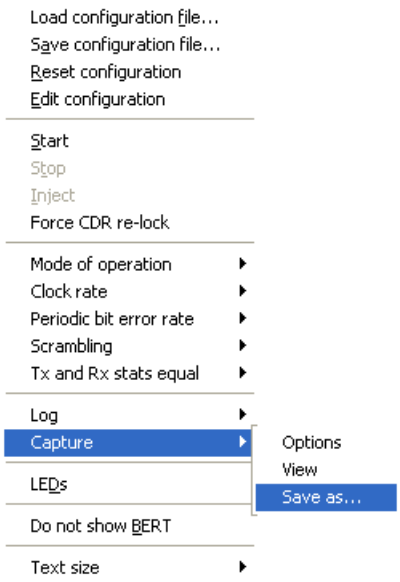
Or:

>> Open the Parameters context menu (Figure 23) and select **Capture > View**.

Or:

>> Click the **Operation** button for the device in either the Parameters Status table or the Ports manager to open the Operation dialog bar. Then click the **Capture** icon.

Figure 23: Capture Menu



Saving a Capture

To save a BERT capture:

>> Open the Parameters context menu (Figure 23) and select **Capture > Save As**.

This command opens a File dialog, Saving BERT capture file, where you can save the capture with a file name you assign to it. The default folder is: Program Files > Viavi > Xgig Maestro > BERT > Captures.

Saving and Naming Captures Automatically

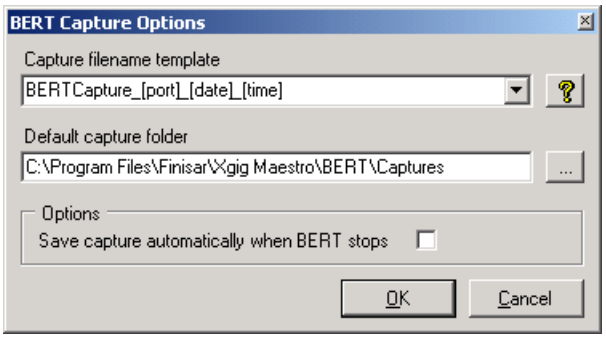
To have capture files automatically named and saved to a specific location:

1 Open the Parameters context menu. (Figure 23).

2 Select **Options**.

This command opens the BERT Capture Options dialog (Figure 24). This dialog allows you to set up how you want the capture files to be automatically named and where you want them saved by default.

Figure 24: BERT Capture Options Dialog



3 Select a capture filename template from the following choices:

- BERTCapture_[port]
- BERTCapture_[port]_[date]_[time]
- BERTCapture_[date]_[time]
- BERTCapture_[date]_[time]_[port]

or, you can type in your own template. The port, date, and time markers are replaced with their corresponding values. Port is displayed as:

```
protocol (FC or GE), chassis name (chassis number in the cascade,
blade number in the chassis, port number on the blade)
```

4 Enter the path to the folder where you want to save the capture file.

You can browse to where you want to save the capture file by clicking ... .

5 Click **OK**.

You have set up the capture filename template and default folder to save the capture.

Captures are saved as `.txt` files.

Note: Capture options are the same for all BERT ports.

Customizing the Appearance of the Maestro/BERT Main Window

You can move and rearrange the individual device tabs on your monitor screen as you prefer. You can also select the information you want to display in the Parameters Status table. In addition, you can select the size of displayed text.

Using the Window Menu

The **Window** menu allows you to arrange the window display:

Layout

Layout offers choices for rearranging the Maestro device tab windows. The Ports manager and Log Manager windows are not affected by this menu selection.

Internal Tabs

Allows you to restore the Maestro main window to its default format.

Internal MDI

Internal multiple document interface (MDI) lets you isolate each device tab as a separate window that you can activate by clicking anywhere on the window.

Show Hidden Windows

Restores any windows you have closed while using the Internal Tabs or Internal MDI display arrangement.

Arrange Icons

Arranges the icons for minimized windows at the bottom of the screen. If an open document window is at the bottom of the screen, some or all of the icons will be underneath this document window and will not be visible.

Cascade

Arranges all open windows in a cascade style from the top, left corner of the window.

1 All Devices

Brings the All Devices tab to the front as the active window. This window displays ports from all active devices (BERT, Jammer, Generator, and Target Emulator).

2 BERT - Bit error rate testing

Brings the BERT device tab to the front as the active window

3 BERT - Latency measurement

Brings the BERT Latency measurement device tab to the front as the active window

4 Jammer

Brings the Jammer device tab to the front as the active window

5 Generator

Brings the Generator device tab to the front as the active window

6 Target Emulator

Brings the Target Emulator device tab to the front as the active window

Tile Horizontally

After selecting **Layout > Internal MDI,** this command opens and aligns the BERT, BERT Latency measurement, Jammer, Generator, and Target Emulator device windows horizontally one over the other.

Tile Vertically

After selecting **Layout > Internal MDI**, this command opens and aligns the BERT, BERT Latency measurement, Jammer, and Generator device windows vertically one next to the other. You can view the individual device windows by dragging the sides out to resize them.

Minimize All Windows

After selecting **Layout > Internal MDI**, this command minimizes all the open windows. You can restore each window, individually, by using the standard window controls on the header or select **Internal Tabs** to restore the Maestro main window to its default format.

Customizing the Parameters Status table in BERT

You can change the appearance of the Parameters Status table by:

- Removing columns
- Resizing columns
- Changing the text size
- Displaying and hiding status table parameters

Removing columns

If you have a number of devices locked, you can remove a column that you do not need to view without unlocking the port or affecting the operation.

To remove a column:

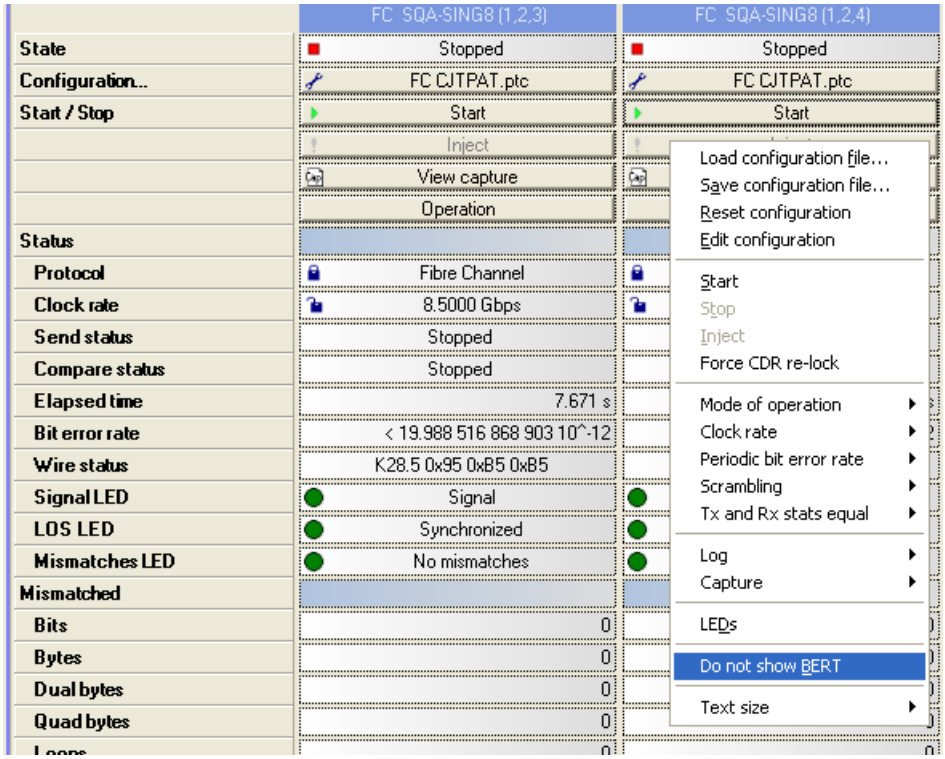
1. Right-click on the specific column you want and open the Parameters context menu.
2. Select **Do not show BERT** (Figure 25).

   Or:

   In the Ports Manager, clear the **Show** check box next to the device you want to remove.

The column is removed, but the device is still locked (“in use”) and displayed in the Ports Manager.

Figure 25: Removing a Device Column



To replace the device column on the Parameters Status table:

>> Click the **Show** check box for the device in the Ports Manager.

Resizing columns

You can resize any of the columns by placing the mouse at the right edge at the top of a column, next to the chassis name. A resizing cursor appears. Hold down the mouse button, and drag the mouse to resize the column.

Changing Text Size

You can choose the text size you want the Parameters Status table or the Ports Manager to display.

Note: You cannot change the text size in the Log Manager.

To change text size:

1. Open the context menu by clicking the right mouse button while the cursor is on the Parameters Status table or the Ports Manager.
2. Select **Text size** (Figure 26).

   You have five choices from which to select.

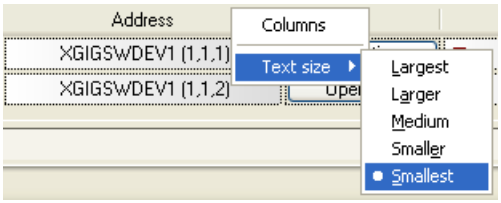
Smallest is the default size.

3 Select the text size you want.

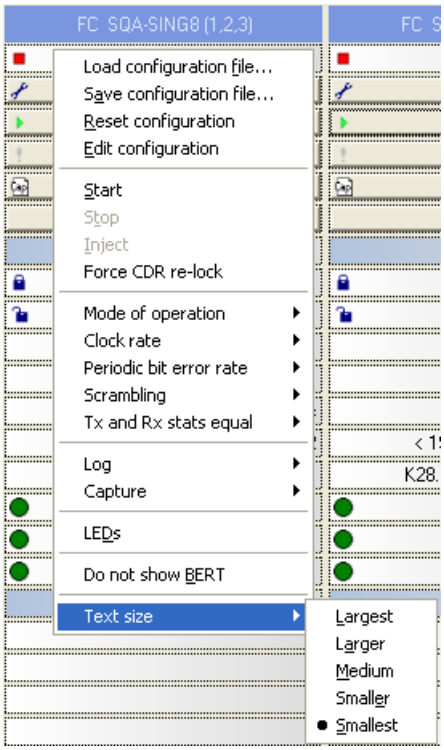
A bullet is displayed next to the current selection.

Figure 26: Text Size Menu

Context menu over Ports manager



Context menu over device parameters status table



Displaying and Hiding Parameters in BERT

You can hide specific parameters on the Parameters Status table to simplify the status tables and show only the information in which you are interested.

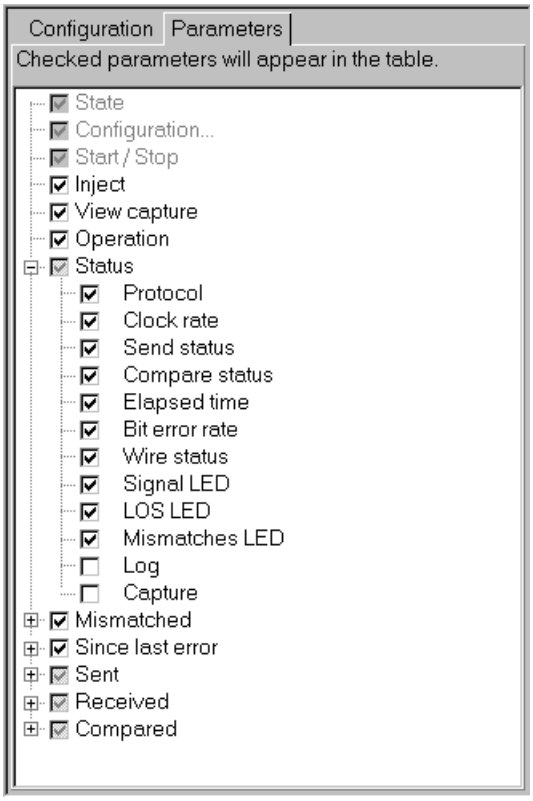
To display or hide parameters on the Parameters Status table:

1 Click the Parameters tab at the top of the Configuration manager pane to switch to the Parameters manager (Figure 27).

You can expand the categories by clicking the plus signs on the left.

The default displays most of the parameters.

Figure 27: BERT Parameters Manager



2 Click check box to set or clear the check mark next to the parameters.

Checked parameters are displayed.

Performing Configuration Tasks in BERT

This section describes how to handle configuration files from the BERT main window.

Loading BERT Configuration Files

You can load a configuration file on a BERT using one of the following methods:

From the Configuration Manger:

>> Drag the configuration file from the list in the Configuration Manager onto the Parameters Status table (column for the device) and release the mouse button.

You can drag configuration files from anywhere, including the list of configuration files in the Configuration Manager on the Xgig Maestro window, the system desktop, or Windows Explorer.

From the Parameters Context Menu:

1. Right-click on the device column to open the Parameters context menu and select **Load configuration file**.

   An Open File dialog is displayed.

2. Navigate to the BERT `.ptc` file that you want to use and click **Open**.

   The file is loaded and its name and parameters are displayed in the device column of the Parameters Status table.

From the Ports Manager:

1. Check the **Select** check box(es) in the Ports Manager for the port(s) you want to use.
2. Click the configuration file you want to load from the Configuration Manager.
3. Click the **Load Configuration to Selected Ports** button  . This button is located in the Ports Manager and in the Configuration Manager. Both have the same function.

You can use the above methods to navigate to a mapped folder and load a configuration file.

You can also use the above methods to load a pattern for BERT from the text script file with the extension `.sct`. See the file BERT Text Script - Readme.txt found in the installation folder for further details.

Saving a BERT Configuration File

To save a BERT configuration file you created or edited:

1. Right-click on the device column in the Parameters Status table to open the Parameters context menu, and select **Save configuration file**.

   A Windows Save dialog is displayed.

2. Navigate to where you want to save the configuration file and assign a name to it.

   Xgig BERT configuration files are saved with a `.ptc` extension.

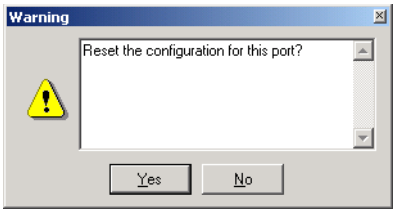
Resetting a BERT Configuration

To clear the configuration from a device:

1 Right-click on the device column in the Parameters Status table to open the Parameters context menu, and select **Reset configuration**.

A warning dialog may be displayed asking you to confirm the configuration reset.

Figure 28: Reset Configuration Warning Dialog



2 Click **Yes** to clear the configuration from the device.

Editing a BERT Configuration

To create a configuration file for a device, you can start from a blank default configuration or edit the configuration after you have loaded a configuration file to the device.

You can open the Configuration window using one of the following methods:

1 Right-click on the device column in the Parameters Status table to open the Parameters context menu.

2 Select **Edit configuration**.

Or:

>> Click the **Configuration** button on the Parameters Status table

This opens the Configuration window for the device that is currently selected. Refer to "Using the BERT Configuration Window" on page 46.

Running a BERT Pattern

After you have configured a BERT device, you can start the operation.

Figure 29: Operation buttons in Ports Manager

>> Right-click on the selected device columns to open the Parameters context menu where the **Start** command is available (**Stop** and **Inject** are grayed out).

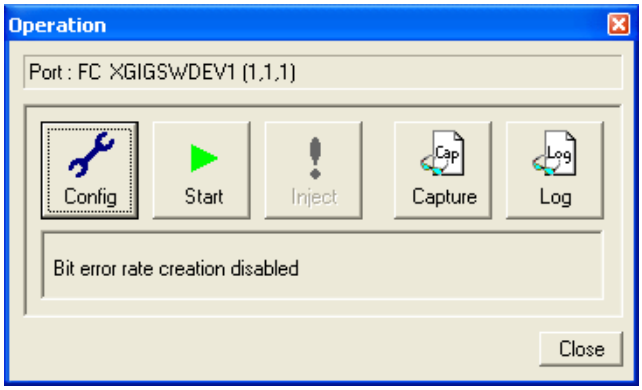
Or:

1 On the Ports manager, in the Operation column, click the **Operation** button for the device.

The Operation dialog is displayed (Figure 30).

2 Click **Start**.

Figure 30: BERT Operation Dialog



Clicking any of the Operation buttons (including **Config**) takes effect on the BERT device that is currently selected (indicated by the name of the device above the buttons).

Start runs a test pattern from the beginning if you click it while the BERT is stopped. When you click **Start**, the Mismatched LEDs and LOS status LEDs are cleared on the Parameters Status table.

Stop causes the BERT to abort running the test pattern and end the test. The BERT always stops sending after it finishes the loop it is sending, and stops comparing after it finishes the loop it is comparing.

Inject inserts a bit error while a test is running. The bit error is placed only among words in the Compare Zone of the defined pattern (except the Start Word). In the 40 bit word, bit 19 or 18 is inverted to create the bit error.

Capture downloads and displays the captured data of the test you have performed.

Log displays the log data for the test you have performed.

Chapter 3

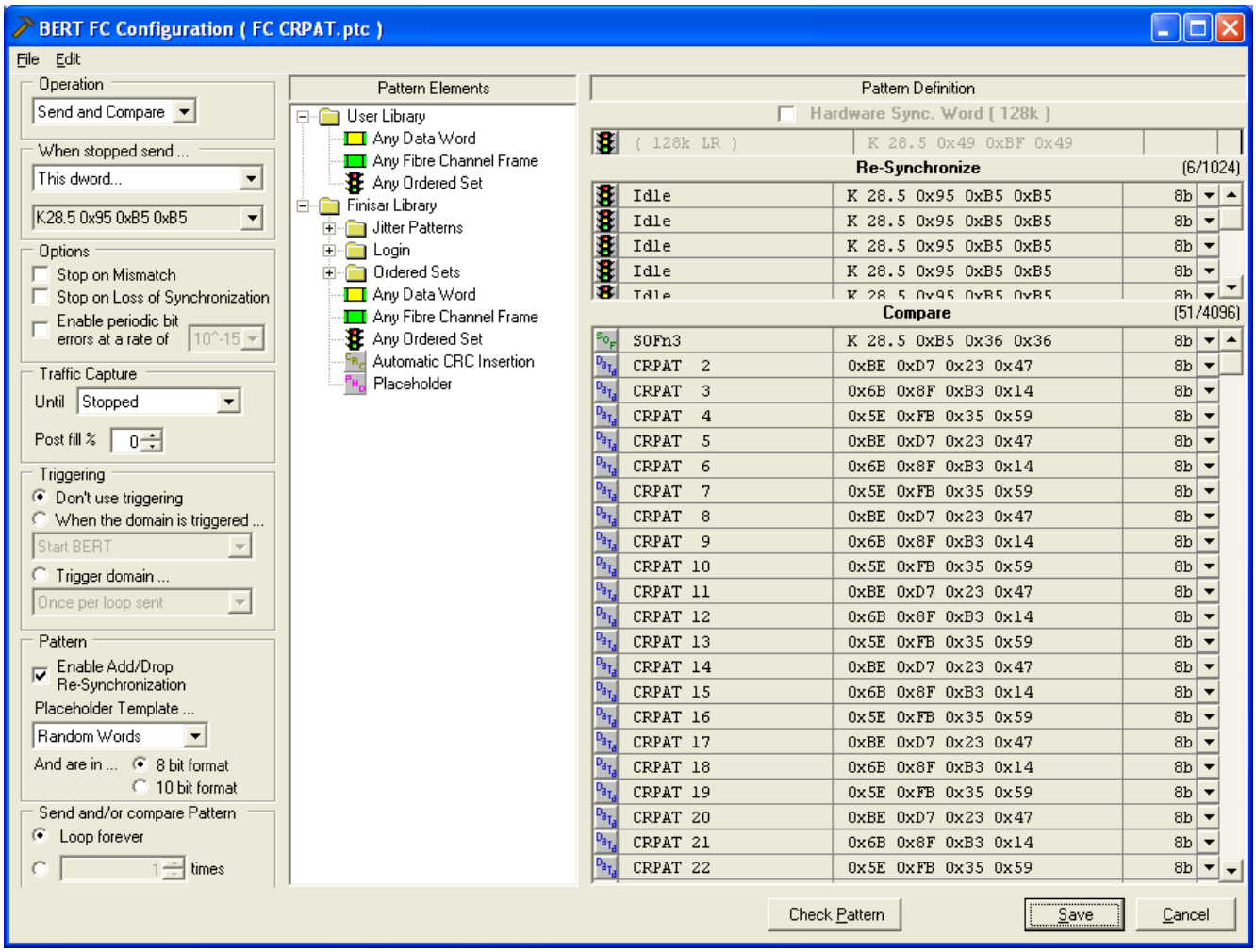
Configuring BERT Settings

In this chapter:

Using the BERT Configuration Window

This section describes each part of the BERT Configuration window (Figure 31) and how to use it.

Figure 31: BERT Configuration Window



Opening the BERT Configuration Window

If you want to create a configuration without assigning ports, on the main window menu bar go to:

File > New BERT configuration > Bit error rate testing > Fibre Channel (Gigabit Ethernet)

Or:

>> Click the **New Configuration** icon at top of the Configuration Manager.

To open this window with hardware assigned to the BERT:

1 On the Port Selection and Domain Setup window, discover the chassis and use ports as BERTs. Refer to the “Using the port Selection and Domain Setup” chapter in the *Maestro Introduction Guide* for details about how to do this.

2 Return to the Xgig Maestro main window and click on a device on the BERT tab, Parameters Status table.

3 Click the **Config** button on the operation bar.

Or:

>> Open the Parameters Status table context menu and select **Edit configuration**.

Or:

>> Click the **Operation** button for the device in the Ports Manager to open the Operation dialog and click the **Config** button.

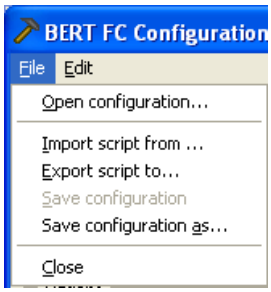
The BERT Configuration window is displayed. From this window you can create your own patterns.

The information in this chapter describes the details of the BERT Configuration window.

Using the Configuration File Menu

The File menu allows you to manipulate the configuration file (Figure 32).

Figure 32: Configuration File Menu



The choices are:

Open Configuration	Open a selected configuration file.
Import Script from	Import the “Re-Synchronize” and “Compare” patterns from a .sct file.
Export Script to	Export and save the “Re-Synchronize” and “Compare” patterns to a .sct file.
Save Configuration	Save the entire configuration to the .ptc file you currently have loaded.
Save Configuration As	Save the entire configuration to a .ptc file with a name you assign to it.
Close	Close the BERT Configuration Window.

The recently-used BERT configuration files appear in the File menu and are loaded when selected.

Note: The .sct files are script files describing bit patterns. You can swap them between configuration files. You can also load a .sct file directly into a BERT device on the Xgig Maestro window.

Using the Configuration Edit Menu

The Edit menu allows you to open the Edit Description dialog (Figure 34).

Figure 33: Configuration Edit Menu

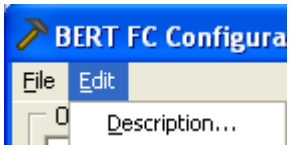
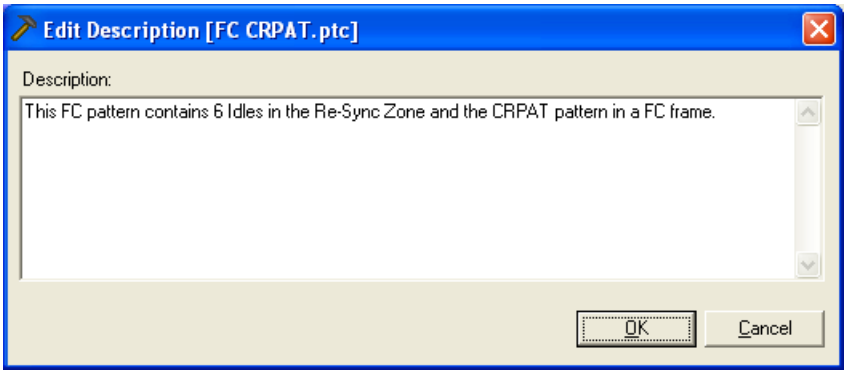


Figure 34: Edit Configuration Description dialog



You can then edit or enter a description for the configuration file and click **OK** to save your changes.

Editing a BERT Configuration

Use step 3 in the previous section to edit a configuration that you have loaded onto the device in the Parameters Status table.

You can also highlight a filename in the Configuration manager and double-click it to display it in the BERT Configuration window.

Operation

Use this drop-down menu on the BERT Configuration window to choose the following Xgig BERT operation mode settings.

Send and Compare Operation

Use the Send and Compare mode, the default setting, when the device under test provides a loop connection such that the bits transmitted return to the Xgig BERT for comparison, or when running two ports in full duplex mode, transmitting to each other.

Send Only Operation

Use this operating mode to transmit “blind.” You can transmit any legal or illegal pattern of bits or disparity to verify performance of a receiver under test. The Xgig BERT receive and compare functions are disabled. This mode is useful for testing the following:

- Data paths for rate divided by 2, 3, 4, 5, etc.
- Phase locked loop extended running 1 or 0 sequence tolerance
- Deserializer comma recognition and synchronization
- Decoding of all legal 10-bit characters
- Decoding of good and bad running disparity situations
- Decoding of all 1024 possible 10-bit characters
- Decoding of all control characters in any byte or bit position
- Noise immunity to non-conforming jitter maximizing patterns
- Remote compare functions on a simplex, very long cable

Using this mode of operation, you can send patterns to another Xgig BERT that is in Compare Only operation mode. You must have the same pattern loaded on both the local and remote Xgig BERT. You must start the Compare Only unit first and then the Send Only unit. At a later time you can reverse the directions.

Compare Only Operation

Use this mode to receive patterns remotely from another Xgig BERT. A remote Xgig BERT sends patterns to the local unit that is in Compare Only operation mode. You must have the same pattern loaded on both the local and remote Xgig BERT. You must start the Compare Only unit first and then start the Send Only unit.

When stopped send...

Use this control to specify what is constantly sent out when the Xgig BERT is in the Stopped state. You can choose:

- Word - Choose a word to be sent continuously, specified in 8-bit or 10-bit mode. The default in Fibre Channel is Idle (K28.5 0x95 0xB5 0xB5) and the default in Gigabit Ethernet is I2/I2 (K28.5 0x50 K28.5 0x50).
- Loss of Synchronization - Transmitter constantly sends ones to simulate Loss of Synchronization.

Note: Whenever you select Loss of Synchronization, the transmitter automatically sends five Hardware Synchronization Words at the end of the very last loop sent, before transitioning back to sending Loss of Sync. This occurs regardless of whether or not the Hardware Sync Word is enabled.

- Passthrough - The port re-times the received traffic and transmits it. This option is only available in Fibre Channel protocol.

Options

The following settings affect Operation.

Stop Operation on Mismatch

When you check this option, the software automatically stops if a mismatch is detected.

Stop Operation on Loss of Synchronization

When you check this option, the software automatically stops if Loss of Synchronization is detected.

Enable Periodic Bit Errors

When you check this option, bit errors are automatically injected into the outgoing traffic within 20 bits of the period specified. You can set the period (10^{-4} to 10^{-15}) here or on the main window, during operation. When calculating the period, only bits in the Compare Zone (except the start word) are counted, and bit errors only occur among these bits. In the 40 bit word, either bit 19 or 18 is inverted to create the bit error.

Traffic Capture

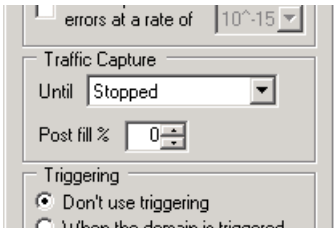
The Xgig BERT includes a capture buffer of 4096, 40-bit words. This buffer captures the last words received at the time of stopping, or the words around a defined trigger point. You can define the trigger point to be the first detected mismatch or a domain trigger in. When sending a finite number of loops, a trigger point automatically occurs at the last word in the last loop, if no other trigger point occurs earlier. The file generated is in ACSII format. You can select options to save the buffer on the Xgig Maestro window. Refer to "Saving a BERT Configuration File" on page 42 and "Using the Capture Commands" on page 35 for more information about these options on the Xgig Maestro window.

To capture traffic:

1 Select from the Traffic Capture Until... drop-down menu to choose when you want the traffic capture to stop.

The default is "Until…/Stopped." This default captures traffic when you start the instrument and continues until you click stop or a "Stop Operation" condition occurs. A Stop Operation condition is defined to stop the whole BERT, not just the Traffic Capture, and is either the first detected mismatch, a domain trigger in, or the last loop of a finite loop setting.

Figure 35: Traffic Capture Settings



When you select "Until…/Mismatch detected," the Traffic Capture stops on the first detected error. By selecting "Until…/Mismatch detected," the trigger word in the Traffic Capture file is the first detected mismatch unless the instrument is stopped before an error is detected. Loss of Sync is considered an error.

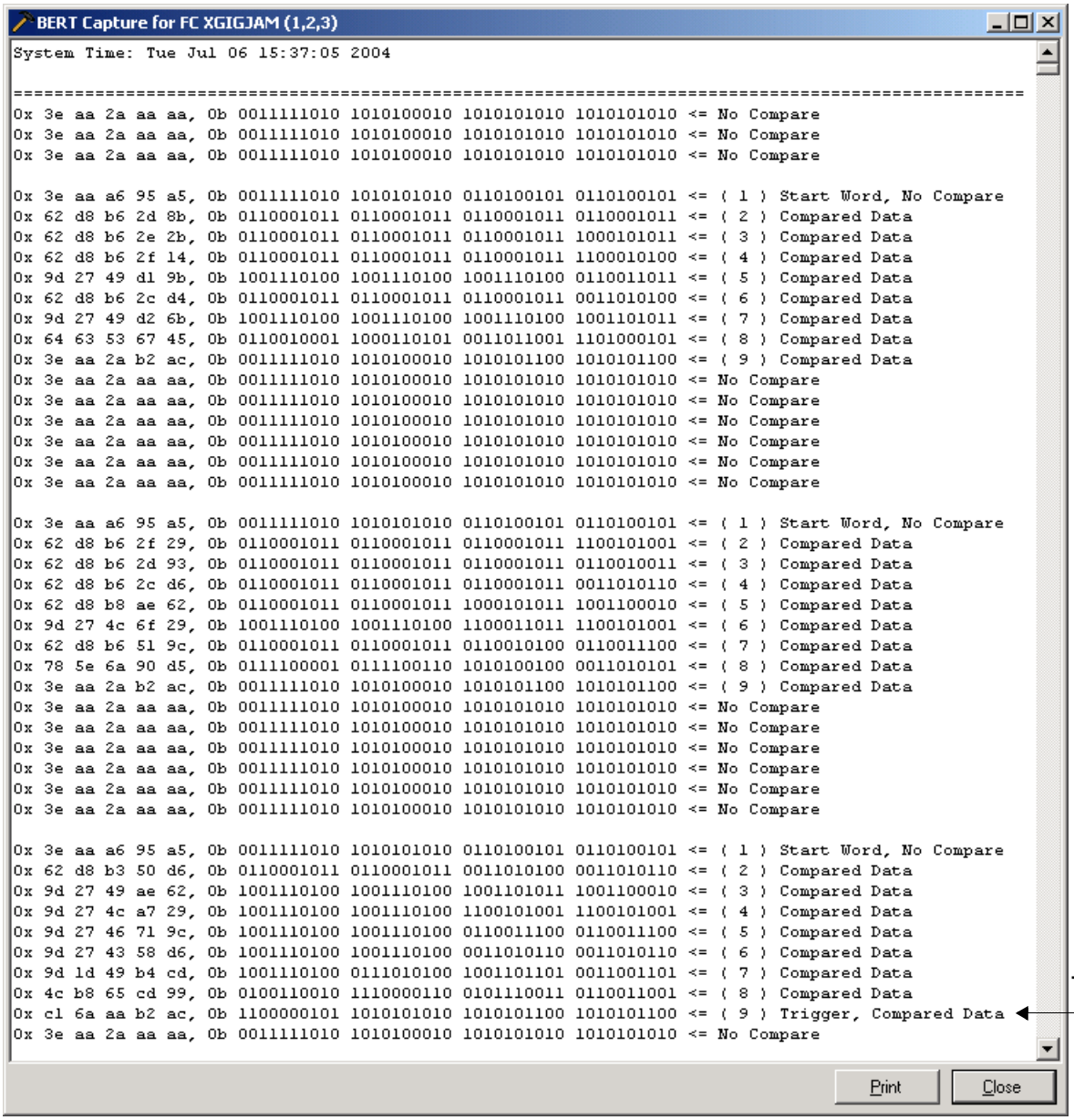
2 Select a post fill percentage value.

This determines the percentage of the data in the Traffic Capture file that will appear after a trigger point in the file (if a trigger occurs). Values range from 0% to 99%.

The Traffic Capture is synchronized to begin when the instrument starts.

Refer to "Using the Capture Commands" on page 35 for additional information about captures.

Figure 36: Example of Traffic Capture Output



Triggering

Use this control to specify the behavior of the triggers to and from the Domain that relate to the BERT.

Don’t use triggering

No triggering is used when you click this radio button.

When the domain is triggered...Start BERT

When you press **Start**, the Status displays “Waiting for trigger” until a trigger in is received.

When the domain is triggered...Stop BERT

When Xgig BERT receives a domain trigger input, the software automatically presses the Stop button. This also creates a trigger for the Traffic Capture file.

Trigger domain...once per loop sent

The domain is triggered at the end of each loop. The trigger pulse is lengthened and passed through the domain with a different clock frequency; therefore, do not use this feature for short repeating loops.

Trigger domain...On traffic capture stop

A trigger out pulse is created when the Traffic Capture is stopped for any reason.

Trigger domain...once per detected mismatch

The domain is triggered for each mismatched quad byte. The trigger is lengthened, therefore, mismatches that are close together do not create a new pulse. A pulse is also created whenever Loss of Sync is detected.

Pattern

This section describes the options in the Pattern field on the Configuration window.

Add/Drop Re-Synchronization disabled (Non-Sync Mode)

To transmit and receive a bit-for-bit matched pattern, make sure that Enable Add/Drop Re-synchronization in the Pattern area of the Configuration window is not checked.

The following activities occur when you use this setting:

1. The Xgig BERT transmits the “stopped” word until you press **Start**.
2. If the Hardware Sync Word is enabled, the Xgig BERT transmits 128k words of the Hardware Synchronization Word (data depends on protocol) allowing the Xgig BERT receiver to synchronize characters and words.
3. The Xgig BERT receiver disables automatic “comma” alignment and uses the present bit relationships for transmit, receive, and compare.

4 The transmitter sends the first through last compare words sequentially, repeating until you click Stop, or until a specified number of loops has been sent.

Note: The first word of the Compare Zone in any mode is called the “Start Word.”

5 The receiver uses the first instance of the Start Word to recognize the beginning of the pattern. Therefore, the very first word must match exactly and is not included in comparison statistics.

6 The receiver counts all receiving statistics after the Start Word is matched once.

If a bit toggles to the opposite state from which it was transmitted, it is counted as a mismatch.

If a bit “disappears” resulting in a slippage of the entire pattern, millions of mismatches are likely to result because the receiver and transmitter are now one bit off and cannot be corrected without being re-synchronized.

Add/Drop Re-Synchronization enabled (Re-Sync Mode)

To repeatedly re-synchronize once each loop, before performing a precise bit comparison (to allow for pattern re-timing), select Enable Add/Drop Re-synchronization in the Pattern area of the Configuration window.

The following activities occur when you use this setting:

1 The Xgig BERT transmits the “stopped” word until you press Start.

2 If the Hardware Sync Word is enabled, the Xgig BERT transmits 128k words of the Hardware Synchronization Word (data depends on protocol) allowing the Xgig BERT receiver to synchronize characters and words.

3 The generator then transmits the re-synchronization word(s)—those in the “Re-Synchronize” area.

It is recommended transmitting at least three of the same re-sync words.

4 The Xgig BERT uses automatic “comma” alignment to realign the received characters and words.

5 The receiver begins counting receive statistics at the first re-sync word.

Note: The first re-sync word should be different from the Hardware Sync Word so that the receiver recognizes the Re-Synchronization zone and starts counting receive statistics.

If the Hardware Sync Word is off, then the receive statistics start from the Start Word on the first loop.

6 Receiver compare is enabled but held off during the re-sync words.

No errors are counted during this time. This allows the transmitter under test to insert or delete (add/drop) re-sync words and re-time the signal sent to the Xgig BERT.

7 Once the Start Word is detected by the receiver, then a bit comparison of the remainder of the pattern is performed (the “Compare Zone”). Note that the Start Word is not counted in the comparison statistics.

Note: Do not use the Start Word in any other place in the pattern, particularly, not in the “Re-sync Zone.”

For example, using six idle words for re-synchronization, and a Compare Zone consisting of a frame with an SOF, 248 data words, a CRC, and an EOF results in 10000 compared bits per loop. Errors in the Idles or SOF are not counted directly. If the received SOF has any mismatched bits, then the receiver skips comparison of that loop and will not record comparison statistics until an SOF match is found.

If a compared bit toggles to the opposite state from which it was transmitted, it is counted as a mismatch.

If a bit “disappears” resulting in a slippage of the entire pattern, hundreds of mismatches are likely to result because the receiver and transmitter are now one bit off for the remainder of the loop. Re-synchronization should correct for minor bit slippage. In the 10000 bit example given, counting the number of mismatched bits and dividing it by 10000 will yield an approximate bit error rate. Remember that 10^{-4} translates to 100% in this example.

Pattern Elements

The Pattern Elements window contains the source templates for creating traffic patterns (Figure 37 and Figure 38). There are frame templates, Ordered Set templates, and special Xgig BERT-specific templates. The template tree that appears in the Pattern Elements window is dependent upon the protocol mode that you set.

Figure 37: Fibre Channel Pattern Element Template Libraries

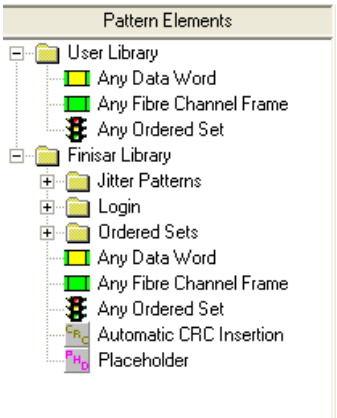
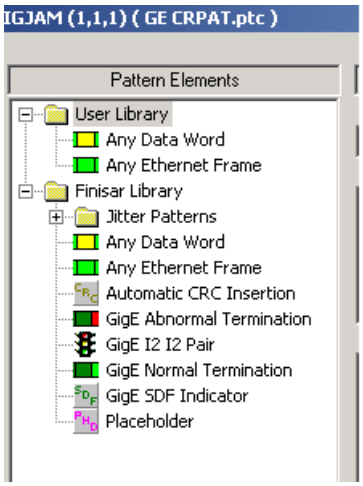


Figure 38: Gigabit Ethernet Pattern Element Template Libraries



You can drag pattern elements within the Pattern Elements window from the read-only Viavi Library to the User Library to edit them.

To edit Pattern Elements in the User Library:

1 Click on a user pattern element, pause, and click again to rename it.

2 Double-click the user element to edit its contents in an editor dialog.

You can also create new folders in the User Library by using the right mouse button.

Ordered Set Template Editor

The Ordered Set Template Editor is only available for the Fibre Channel Ordered Set Templates.

To open the Template Editor dialog:

>> Double-click on an Ordered Set Template in the User Library folder of the Pattern Elements window.

Frame Template Editor

To open the Frame Template Editor dialog (Figure 39 and Figure 40):

>> Double-click on a Frame Template in the User Library folder of the Pattern Elements window.

Figure 39: Fibre Channel Any Frame Template Editor Dialog

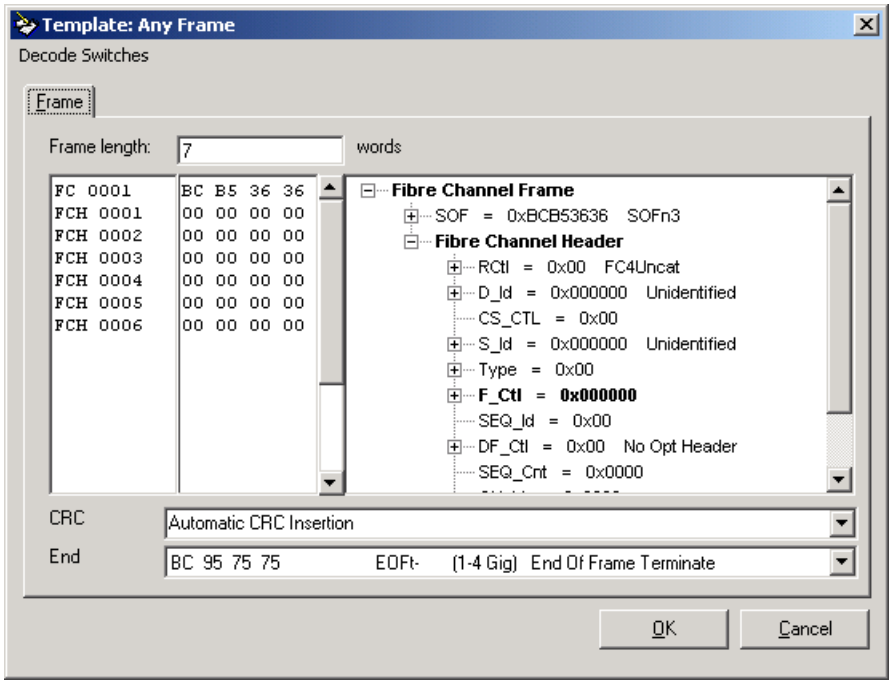
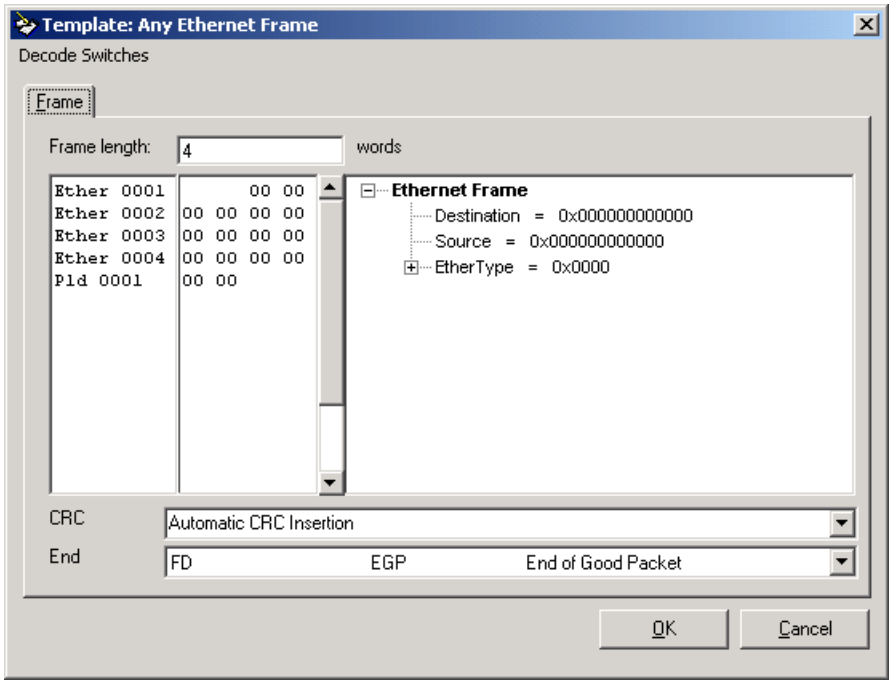


Figure 40: Gigabit Ethernet Any Frame Template Editor Dialog



Decode Switches Menu

The Decode Switches menu lets you select the manner in which you want to display the bytes in a frame. The Decode Switches menu only appears when there is a payload specified (set the number of words in the Frame length field to be greater than the number of words in the header.) Only switches relevant to the current template being edited would appear. There are also contextual switches to further decode responses and data frame templates. For further information about decode switches, refer to the *Xgig Analyzer User's Guide*.

Frame Length

You can enter a legal frame length in words in the Frame Length field at the top of the editor dialog.

Columns

The editor has three columns:

- Word pointers

  The left column is a named word pointer. You can select pointers, copy, cut, and paste them. Word values move along with the pointers.

  — Fibre Channel frames start with an SOF, have an option VSAN header of 2 words (VSAN 1 and 2), follow on with six header words (FCH1-6), continue with payload words P001-P528, then a CRC, and an EOF.

  — Gigabit Ethernet frames start with an S Ordered Set, six preamble bytes, and 1 SDF byte (not shown in the template), followed by 14 header bytes (Ether 0001-0004), payload words Pld 0001-0376, then a CRC and an EOF.

- Word value in hex

  The center column is the word value. These are entered in hexadecimal. All words are D characters, except the K character at the first byte of the SOF word in Fibre Channel, and the K character at the S Ordered Set at the beginning of the frame (not shown in the template).

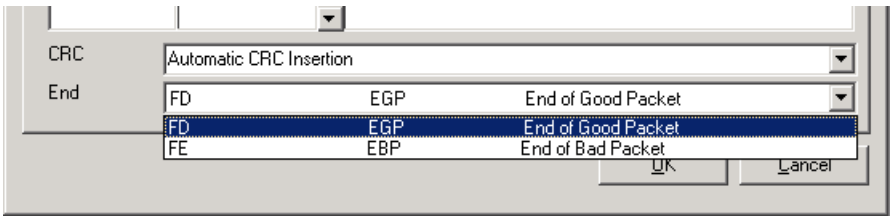
- Protocol decode string

  The right column contains translations of the hex words in the frame into protocol decoded strings. Use the mouse cursor to click on the + symbol, to display a sub-list of possible decode values. You can select one of the elements in the list and the hex word updates to reflect the appropriate bit values.

CRC and End Word Controls

At the bottom of the editor are the CRC and End word controls (Figure 41). You can type a CRC value or let Automatic CRC Insertion send the valid CRC for the frame.

Figure 41: CRC and End Word Controls



Xgig BERT-Specific Templates

Pattern Elements include some Xgig BERT specific templates. These are specialized template elements that you can only use with the Xgig BERT. Some of these templates are protocol-specific, some are not. The protocol-specific templates are described in the next section. The templates that are not protocol-specific are the Automatic CRC, the Any Data Word, and the Placeholder.

Automatic CRC Generation and Insertion

Fibre Channel and Gigabit Ethernet use a 32-bit cyclic redundancy check (CRC). To insert a dynamically computed CRC, you need to use two Xgig BERT specific templates. One is a protocol-specific SOF or SDF Insertion element (green SOF or SDF icon), the other is the protocol independent Automatic CRC element (yellow CRC icon). The hardware recognizes an Xgig BERT specific SOF or SDF Insertion element and starts a CRC-32 calculation with the word immediately after the element. The calculation continues until the Automatic CRC Insertion element is found, and the CRC is inserted on that word. The CRC is automatically calculated for the entire frame including placeholder entries. You should place the CRC element just prior to the frame terminator.

Important: All entries between the SOF/SDF template and the automatic CRC template must not have control (K) characters, and must be 8-bit entries; 10-bit entries are not handled correctly by CRC.

An SOF or SDF that is not a special template containing a green SDF or SOF icon will not work with the automatic CRC calculator.

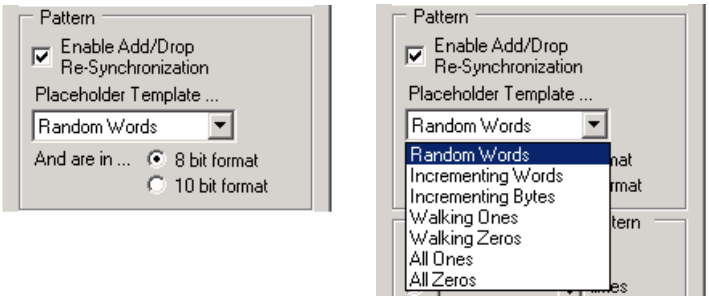
Any Data Word

The Any Data Word template is a one word element that can be used to create an 8-bit data word that has no K-char bits. Once this template is moved to the Pattern Definition window, you can change the word to 10 bit mode, or you can enable K-char bits.

Placeholder

The third element, Placeholder, represents a hardware-based counter/accumulator register. You can include automatic Placeholder words along with the pattern templates. Figure 42 shows the Placeholder Template menu.

Figure 42: Placeholder Template menu



Using the Placeholder Element

To use the Placeholder element, select the one hardware counter type you want to use throughout the pattern. For example, select Incrementing Words, 8-bit Format. Each time you drag a Placeholder element into the pattern, it is pointing to the one Incrementing Word counter in hardware. Every time the pattern encounters this Placeholder, the present value is used and the counter incremented. The same register might be listed repeatedly, for example, four successive Placeholder copies of “Incrementing Bytes.” This results in the pattern transmitting the proper disparity and 10-bit values for the hex characters listed in Table 6.

Table 6: Four Placeholder 8-bit Values for Hex Characters

0x00	0x00	0x00	0x00
0x01	0x01	0x01	0x01
0x02	0x02	0x02	0x02
0x03	0x03	0x03	0x03
(end of first pass through the pattern)			
0x04	0x04	0x04	0x04
0x05	0x05	0x05	0x05
0x06	0x06	0x06	0x06
0x07	0x07	0x07	0x07
(end of second pass through the pattern)			
0x08	0x08	0x08	0x08
: : : : : : : : : : : : : : : : : : : :			
0xFF	0xFF	0xFF	0xFF
(end of sixty fourth pass through the pattern)			
0x00	0x00	0x00	0x00

If you change the Placeholder Template setting, all Placeholders in the pattern are affected and when the pattern is restarted, it will use the new setting each time a Placeholder is encountered.

You cannot use the Placeholder as the first compare word. You can use it as the last compare word.

8-Bit Placeholders

The 8-bit Placeholders are transmitted with proper disparity and translated to 10-bit from the registers described in Table 7.

Table 7: 8-bit Placeholder Registers

Register	Description	Initial Value
Random Words	32 Bit Pseudo-Random left shift register with bits 31, 30, 15 and 1NOT XOR'd into the least significant bit.	0x00 00 00 00
Incrementing Bytes	1 Byte Counter x 4, counts 0x00 to 0xFF and then repeats; all bytes are equal.	0x00 00 00 00
Incrementing Words	32-Bit Incrementing counter, counts from 0x00 00 00 00 to 0xFF FF FF FF, then wraps to 0x00 00 00 00 and continues.	0x00 00 00 00
Walking Ones	32-Bit left shift register, shifts from 0x00 00 00 01 to 0x80 00 00 00, then repeats	0x00 00 00 01
Walking Zeros	32-Bit left shift register, shifts from 0xFF FF FF FE to 0x7F FF FF FF, then repeats.	0xFF FF FF FE
All Ones	Static 1's.	
All Zeros	Static 0's.	

10-Bit Placeholders

The 10-bit Placeholders are transmitted without regard for proper disparity directly from the registers described in Table 8.

Table 8: 10-bit Placeholder Registers

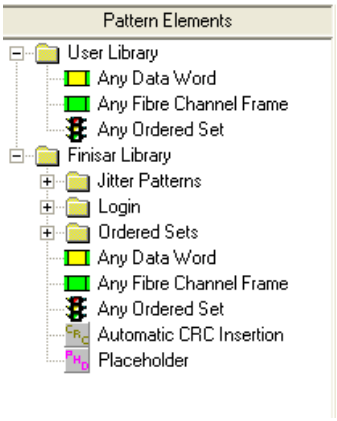
Register	Description	Initial Value
Random Words	40-Bit Pseudo-Random left shift register with bits 31, 30, 15 and 1NOT XOR'd into the least significant bit.	0x00 00 00 00 00
Incrementing Bytes	10-Bit Counter x 4, counts 0x000 to 0x3FF and then repeats; all characters are equal.	0x00 00 00 00 00
Incrementing Words	40-Bit Incrementing counter, counts from 0x00 00 00 00 00 to 0xFF FF FF FF FF, then wraps to 0, then continues.	0x00 00 00 00 00
Walking Ones	40-Bit left shift register, shifts from 0x00 00 00 00 01 to 0x80 00 00 00 00, then repeats.	0x00 00 00 00 01
Walking Zeros	40 Bit left shift register, shifts from 0xFF FF FF FF FE to 0x7F FF FF FF FF, then repeats.	0xFF FF FF FF FE
All Ones	Static 1's.	
All Zeros	Static 0's.	

Note: You can only use one representation for Placeholders at a time. When you select Incrementing Words, an incrementing value is placed at each Placeholder location in the pattern.

Xgig BERT-Specific Protocol-Specific Templates

Pattern Elements include some Xgig BERT-specific templates that are only available in a certain protocol mode (Figure 43 and Figure 44). These templates are the SOF Indicator, the SDF Indicator, the GigE Normal Termination Indicator, and the GigE Abnormal Termination Indicator.

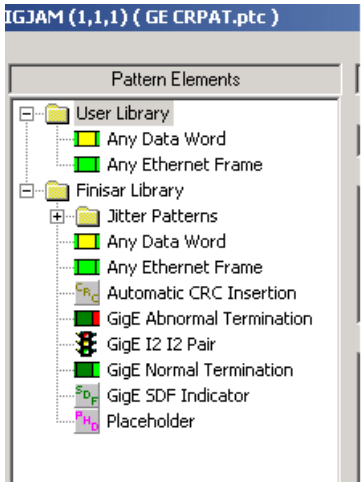
Figure 43: Fibre Channel Pattern Elements



SOF Indicator

The SOF indicator shows a start of frame and resets the automatic CRC calculator in the Fibre Channel Protocol. You edit this template the same way you edit the Fibre Channel Ordered Set Templates. The Viavi Template library contains an SOF indicator for each type of Fibre Channel SOF (for example: SOFi3, SOFn3, etc.). You can also create your own SOF template or edit the data in the Pattern Definition. The SOF indicator element enables the hardware based automatic CRC calculator to begin with the word following the four byte SOF indicator. It is not necessary for any byte in the SOF indicator to be a control (K) character and no bytes of the SOF Indicator are included in CRC calculation.

Figure 44: Gigabit Ethernet Pattern Elements



SDF Indicator

The SDF indicator is usually the second word of a frame and resets the automatic CRC calculator in the Gigabit Ethernet Protocol. The default data is 0x55 0x55 0x55 0xD5. A data word of K27.7 0x55 0x55 0x55 should be put before this template for a proper frame beginning. The SDF indicator element enables the hardware based automatic CRC calculator to begin with the word following the four byte SDF Indicator. It is not necessary for any byte in the SDF Indicator to be a control (K) character and no bytes of the SDF Indicator are included in CRC calculation.

Gigabit Ethernet Normal Termination Indicator

The Gigabit Ethernet Normal Termination Indicator is used to terminate a Gigabit Ethernet frame, and should be placed after the CRC word. The data contents are T/R/I1 or T/R/I2 (K29.7 K23.7 K28.5 0xC5 or 0x50). You cannot edit this data. The hardware automatically chooses between I1 and I2, depending on the incoming current running disparity (if positive, I1 is used, if negative, I2).

Gigabit Ethernet Abnormal Termination Indicator

The Gigabit Ethernet Abnormal Termination Indicator is used to terminate a Gigabit Ethernet frame; you should place it after the CRC word. The data contents are V/R/I1 or V/R/I2 (K30.7 K23.7 K28.5 0xC5 or 0x50). You cannot edit this data. The hardware automatically chooses between I1 and I2, depending on the incoming current running disparity (if positive, I1 is used, if negative, I2).

Using Pattern Definition

The Pattern Definition window is where you create your pattern. The Hardware Sync Word is always shown at the top, and the Compare Zone is always at the bottom. In between these zones is the Re-Sync Zone, if Re-Sync Mode is enabled.

You can place up to 1024 words in the Re-sync Zone and 4096 words in the Compare Zone.

Caution: In Gigabit Ethernet mode, I2 Ordered Sets must be present just before the Start Word to assist in alignment. Make sure to always have I2 Ordered Sets in the Re-Sync Zone. If a Re-Sync Zone is not present and the Hardware Sync Word is turned off, be sure to set the “When stopped send...” word to I2/I2**.**

To turn the Hardware Sync Word on and off:

>> Click the check box.

Notice that if you do not use the Hardware Sync Word, then all the receive statistics begin with the Start Word, regardless of whether there is a Re-Sync Zone or not. For the first loop, statistics are only taken for the Compare Zone. For subsequent loops, statistics will include all received data as normal.

Creating and Organizing Words

To populate the Re-Sync Zone and Compare Zone:

>> Drag and drop templates from the Pattern Elements window.

When you drag and drop a Frame Template, it is automatically broken up into its constituent words.

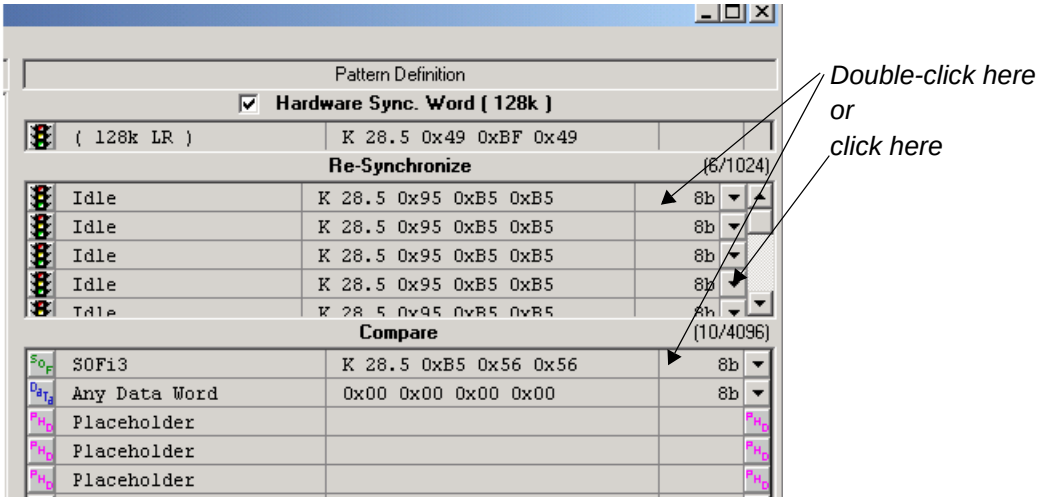
Another way to create and organize words is to use standard cut, copy, and paste commands (only within a single zone at a time).

To edit words in the Re-Sync Zone and Compare Zone, use the Pattern Word Editor.

Using the Pattern Word Editor

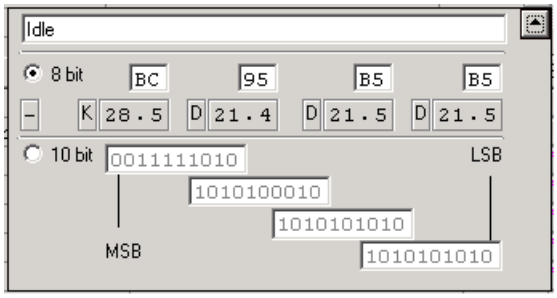
To open the pattern word editor, double-click on an entry in the Re-Synchronize or Compare windows on the right side of the configuration screen (Figure 45) or click on a down arrow on the right side of the entry.

Figure 45: Opening the Pattern Word Editor



The pattern word editor dialog is displayed (Figure 46).

Figure 46: Pattern Word Editor Dialog



This editor allows you to define the actual 10-bit value to be transmitted or the 8-bit value that the hardware encodes to the correct 10-bit translation, based on the running disparity.

Use the following guidelines when you edit words in a pattern:

- For 8-bit mode, use the + or - button to select the incoming disparity for the 10-bit conversion. For 10-bit mode, the + or - has no function.
- You must use 8-bit mode for automatic CRC calculation.

- Note that the translated 10-bit values are ignorant of disparity. You might need to manually pick the opposite starting disparity value by inverting the 10-bit value to follow disparity rules.
- You can enter a name for this word at the top of the editor.
- After selecting 8-bit, you can enter hex values and click on the “D” or “K” to toggle it to the other state.
- If you select 10-bit, you can only enter 1s and 0s. Illegal characters are “??” in hex translations in 8-bit.

Important: Watch out for disparity issues and receiver restrictions if you enter 10-bit values. 10-bit values are always transmitted “As Is;” whereas, 8-bit values are transmitted using correctly generated disparity. 8-bit Ordered Sets are transmitted following the appropriate protocol-specific disparity rules, regardless of the current running disparity.

- The Pattern Word Editor does not allow you to edit the following templates:
  - Automatic CRC
  - Placeholder
  - GigE Normal Termination Indicator
  - GigE Abnormal Termination Indicator

Send and/or compare Patterns... (Finite Loop Setting)

Use this control to send and/or compare the pattern a finite number of times. You can select:

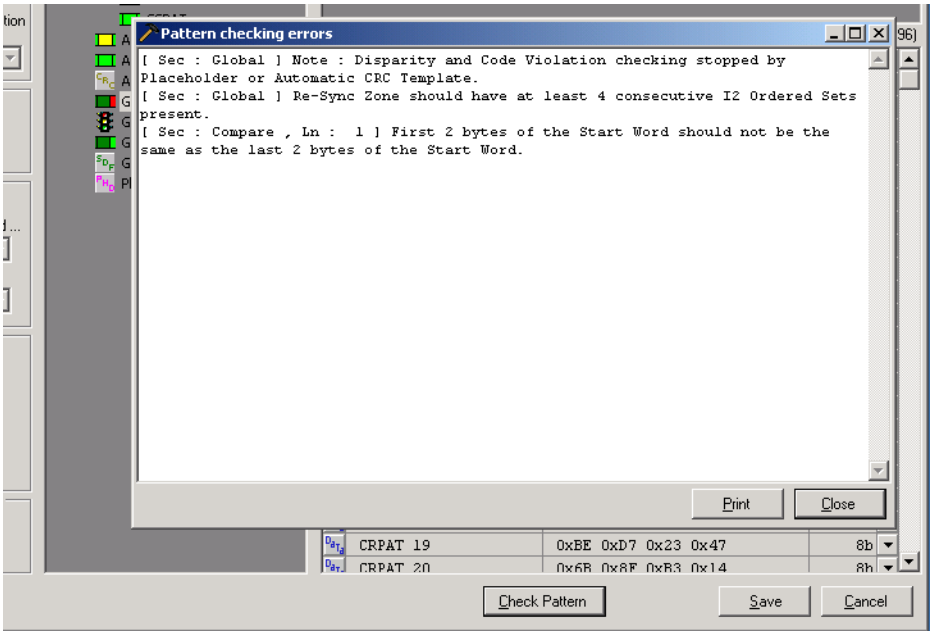
- Looping forever
- A specified number from 1 to 4294967295

When you use a finite number and click **Start**, the Xgig BERT runs until the number of loops are complete; then the unit automatically returns to the stopped state. Additionally, a Traffic Capture “trigger” condition is created at the last word of the last loop.

Check Pattern

You can check your pattern in Xgig BERT for code violations, disparity errors, and warnings that might cause your pattern to fail. After you define a pattern, click the **Check Pattern** button (Figure 47).

Figure 47: Check Pattern Button



Xgig BERT highlights disparity errors and code errors in yellow and reports their line number and byte position. Note that byte 0 refers to the msb on the far left, while byte 3 is on the far right. In addition, it displays the following warnings when it detects pattern errors:

General Warnings

The following warnings are displayed for errors that occur in either protocol:

`Start Word should not be used elsewhere in pattern.`

`Start Word cannot be a Placeholder.`

`Placeholder cannot be put into the Re-Sync Zone.`

`Start Word cannot be an auto CRC template.`

`CRC template cannot be put into Re-Sync Zone.`

`Compare function will not be useful with 10 bit Placeholders in pattern.`

`Unaligned comma character may cause Compare function to lose sync with pattern.`

`Compare Zone should be longer than 8 words to allow for 8 clock width TTL-out pulsing.`

`Start Word should not be an 8 bit EOF.`

`Compare Zone cannot be empty.`

Fibre Channel Mode Warnings

The following warnings are only displayed in Fibre Channel Mode:

```
First word of Re-Sync or Compare Zones cannot equal Hardware Sync Word.

10-bit data is not allowed between SOF template and auto CRC template.

K-Char characters are not allowed between SOF template and auto CRC
template.

SOF and auto CRC templates must be in pairs where SOF comes before auto
CRC.

Auto CRC template found without partner SOF template.

SOF template and auto CRC template must have at least 1 word between
them.

SOF template cannot put into the Re-Sync Zone.

Re-Sync Zone must have at least 3 consecutive Ordered Sets present that
may be added or dropped.

Compare Zone should not contain Ordered Sets that may be added or
dropped.
```

Gigabit Ethernet Mode Warnings

The following warnings are only displayed in Gigabit Ethernet Mode:

```
First word of Compare Zone cannot equal Hardware Sync Word.

First 2 bytes of the Start Word should not be the same as the last 2
bytes of the Start Word.

10 bit data is not allowed between SDF template and auto CRC template.

K-Char characters are not allowed between SDF template and auto CRC
template.

SDF and auto CRC templates must be in pairs where SDF comes before auto
CRC.

Auto CRC template found without partner SDF template.

SDF template and auto CRC template must have at least 1 word between
them.

Re-Sync Zone must have at least 4 consecutive I2 Ordered Sets present.

Compare Zone must not have I2 Ordered Sets present, because other devices
may add or drop them.

Start Word cannot be a T/R/IX nor V/R/IX template.
```

You can send your pattern to a device, but if it contains a warning, the results can be unpredictable. Disparity errors do not affect an instrument's performance except as defined by bit DC bias requirements.

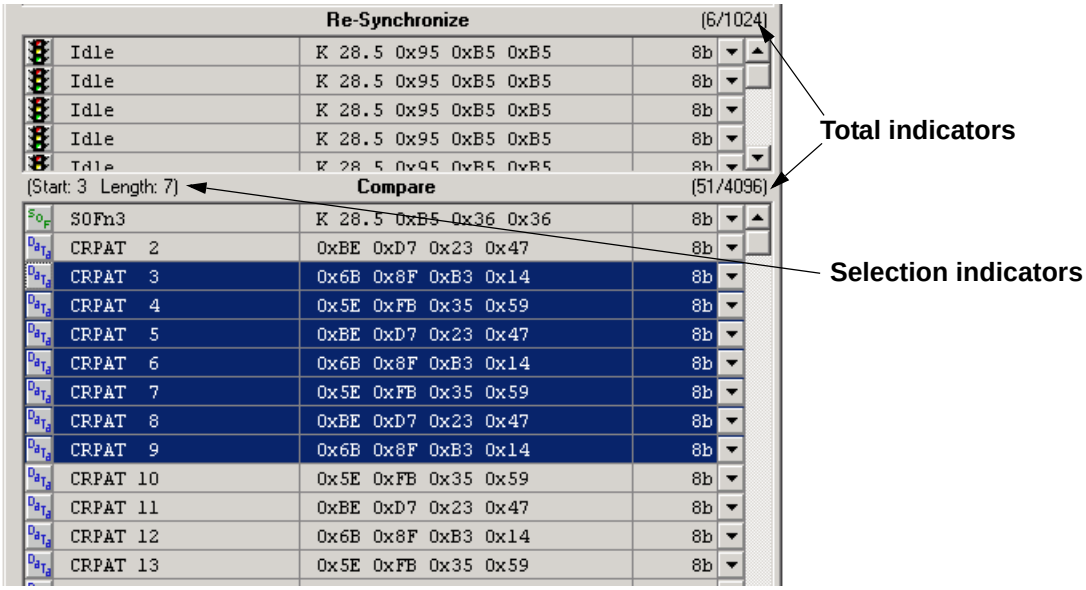
Pattern Indicators

The BERT Configuration window has indicators that show current selection information for the Re-Synchronize Zone and Compare Zone. They are located in the header of each zone (Figure 48).

The selection indicators, on the left side of the header, show the current selection point within a particular pattern window (Start) and the number of items selected (Length). These indicators only appear for the zone you currently have selected (Re-Sync or Compare).

The total indicator on the right of the header displays the number of words used in the pattern and the maximum number of words allowed.

Figure 48: Pattern Indicators



Protocol-Specific Features

This section describes the protocol-specific features for BERT mode.

Fibre Channel

Xgig BERT supports the Fibre Channel protocol as follows:

- The Hardware Sync Word (128k sent at beginning of pattern) is LR (K28.5 0x49 0xBF 0x49)
- The default for the “stopped word” is Idle (K28.5 0x95 0xB5 0xB5)
- The default speed is 2.1250 Gbps for a 2.1250 Gbps blade, 4.2500 Gbps for a 4.2500 Gbps blade and 8.5000 Gbps for an 8.5000 Gbps blade
- The Ordered Set templates in the Pattern Elements window are editable as described previously
- In Re-Sync Mode, received comma characters are aligned to byte 0 (msb) for comparison. (Be sure to only put comma characters in the left-most byte.)
- 8b Ordered Sets are always sent with the proper negative incoming disparity (except EOFs)
- 8b EOFs are always corrected to the right code on-the-fly in hardware according to the running disparity
- In Re-Sync Mode, there should be at least 3 equal consecutive Ordered Sets in the Re-Sync Zone so that other devices may add or drop to re-time
- Xgig BERT-specific SOF template indicators are available
- To use the Automatic CRC template, you should place an SOF indicator template (green icon) at the beginning of the frame, and an Automatic CRC template at the end after the payload, before the EOF
- To use Fibre Channel Frame Scrambling, you should use an SOF indicator template at the beginning of the frame. Scrambling will begin on the next word and continue until a word containing a K character (usually EOF). Scrambling is enabled or disabled for each BERT port in the Parameters context menu on the BERT tab.

Gigabit Ethernet

Xgig BERT supports the Gigabit Ethernet protocol as follows:

- The Hardware Sync Word (128k sent at beginning of pattern) is I2/I2 (K28.5 0x50 K28.5 0x50)
- The default for the “stopped word” is I2/I2 (K28.5 0x50 K28.5 0x50)
- The default speed is 1.25 Gbps
- The Ordered Set templates in the Pattern Elements window are not editable (until you put them into the pattern)
- In Re-Sync Mode, received comma characters are aligned to byte 0 (msb) and byte 2 for comparison. (Be sure to only put comma characters in the left- most byte and the third from left byte.)

- 8b I2 Ordered Sets are always sent with the proper negative incoming disparity. Note that the Check Pattern feature does not include this in its disparity rules.
- 8b I1 Ordered Sets are always sent with the proper positive incoming disparity. Note that the Check Pattern feature does not include this in its disparity rules.
- The Gigabit Ethernet Normal Terminator and Gigabit Ethernet Abnormal Terminator templates automatically choose in hardware between I1 and I2 to terminate the frame with the correct negative disparity.
- In Re-Sync Mode, there should be at least four equal consecutive Ordered Sets in the Re-sync Zone so that other devices can add or drop to re-time (for example, 2 I2/I2 pairs).
- When you use the Automatic CRC template, you should place an SDF indicator template (green icon) at the beginning of the frame, and an Automatic CRC template at the end after the payload, before the frame terminator template.
- The SDF indicator template should usually be the second word of the frame. A word containing the S Ordered Set and three preamble characters (K27.7 0x55 0x55 0x55) should usually be the first word in the frame.
- In Re-Sync mode with the Hardware Sync Word on, if you use I2/I2 as the words in the Re-Sync Zone, when the receiver receives the first loop it will not count the Re-Sync words in the statistics (only for the first loop). This is because the receiver looks for the first word that is different from the Hardware Sync Word (I2/I2) to start accumulating statistics.
- In Re-Sync Mode, the receiver constantly looks for a match of the first two bytes of the Start Word, and aligns the data stream to the msb position upon any match, for comparison purposes. Therefore, you should never use the first two bytes of the Start Word anywhere else in the pattern. In Non-Sync Mode, the alignment is only performed once at the beginning of the first loop received; so the pattern restriction does not apply.
- Xgig BERT specific templates available for Gigabit Ethernet:
  - SDF Indicator
  - GigE Normal Termination Indicator
  - GigE Abnormal Termination Indicator

Cancel and Save Buttons

These buttons control the updating of the entire Configuration window and allow you to save the settings you make.

Cancel

Closes the Configuration window and returns to the main window. All changes that you made since the last time you opened the Configuration window are lost.

Save

If you are in edit only mode, without assigned hardware, the Configuration window displays a **Save** button. Click this button to save the configuration you have created or edited.

BERT Configuration Files

You can use configuration files (with the extension .`ptc`) to save all the contents of the Configuration window. The current configuration file name is displayed in the Parameters Status table on the Xgig Maestro window and on the title bar in the Configuration window. For information about how to load a configuration file, save a configuration file, reset a configuration, or edit a configuration file, see page “Loading BERT Configuration Files” on page 42.

Chapter 4

Configuring Latency Settings

In this chapter:

Xgig BERT provides latency measurement by sending out frames and measuring the time they take to return to the BERT. The frame pattern is similar to a pattern you can create in BERT mode, but, for the most part, you cannot edit it. The pattern uses the Hardware Sync Word and a Re-Sync Zone with Idles for the appropriate protocol. The Compare Zone (no bit comparison occurs) contains one protocol-specific, dynamically changing frame.

This chapter describes how to use this feature.

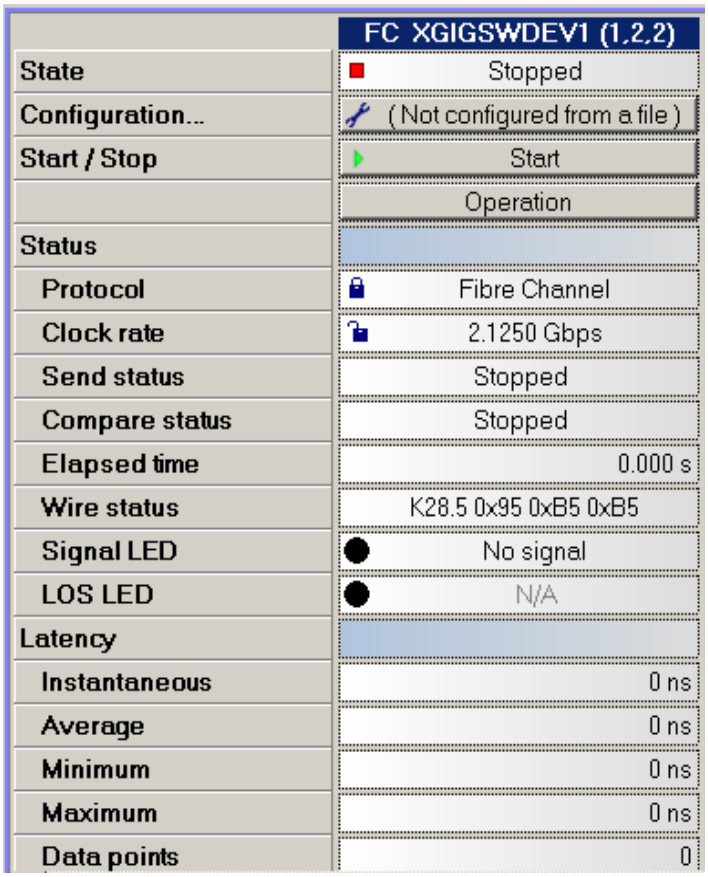
To enable the Latency mode:

1 Select a port and lock it port as a BERT on the Port Selection and Domain Setup window.

2 On the BERT tab, right-click on the port to open the Parameters context menu and select **Mode of operation > Latency mode**.

The Latency tab on the Xgig Maestro window is displayed (Figure 49).

Figure 49: Latency Tab



Using the BERT Latency Configuration Window

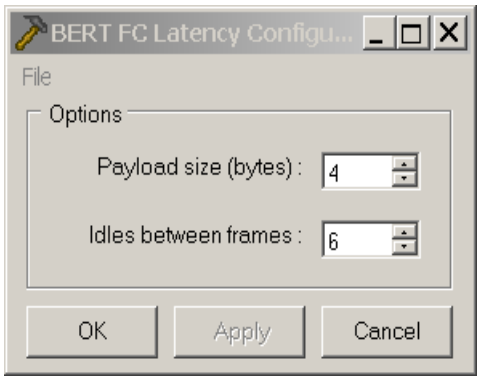
To configure Latency:

1 Be sure the device you want to configure is selected in the Parameters Status table.

2 Click the Configuration File button (Figure 49).

The Latency Configuration window is displayed (Figure 50).

Figure 50: Latency Configuration Window



3 Set the following to configure latency.

In the Options area:

- **Payload size**

  Controls the number of bytes in the payload of the frame sent. Payload is counted by 4 bytes.

  For Fibre Channel, the minimum is 4, maximum is 2112.

  For Gigabit Ethernet, the minimum is 10, the maximum is 4066.

- **Idles between frames**

  Controls the number of Idle characters between frames. Idles are counted by 1 in Fibre Channel and by 2 in Gigabit Ethernet.

  For Fibre Channel, the minimum is 6 and maximum is 1024.

  For Gigabit Ethernet, the minimum is 5, the maximum is 2049.

4 Click **Save** or **Cancel**.

These two buttons control updating for the entire Configuration window.

Save

Saves all the Configuration window settings.

Cancel

Closes the Configuration window and returns to the main window. All changes that you made since the last time you opened the Configuration window and clicked **Apply** are lost.

Saving Configuration Files

When you save a configuration file, the file contains the settings from the BERT tab and the Latency tab. You can save the contents of the Configuration window to file names you specify. For more information about configuration files, refer to “Saving a BERT Configuration File” on page 42.

Protocol-Specific Features

This section describes the protocol-specific features for Latency mode:

Fibre Channel

Xgig BERT supports the Fibre Channel protocol as follows:

- The Hardware Sync Word (128k sent at beginning of pattern) is LR (K28.5 0x49 0xBF 0x49).
- The default for the “stopped word” is Idle (K28.5 0x95 0xB5 0xB5).
- The default speed is 2.1250 Gbps for a 2.1250 Gbps blade, 4.2500 Gbps for a 4.2500 Gbps blade, and 8.5000 Gbps for an 8.5000 Gbps blade.
- The frame contains SOFn3, six header words, a user-defined payload length, a good CRC, and EOFt.

Gigabit Ethernet

Xgig BERT supports the Gigabit Ethernet protocol as follows:

- The Hardware Sync Word (128k sent at beginning of pattern) is I2/I2 (K28.5 0x50 K28.5 0x50)
- The default for the “stopped word” is I2/I2 (K28.5 0x50 K28.5 0x50)
- The default speed is 1.25 Gbps.
- The frame contains 14 header bytes, a user-defined payload length, a good CRC, and a normal frame termination.

Chapter 5

Using the Latency Tab

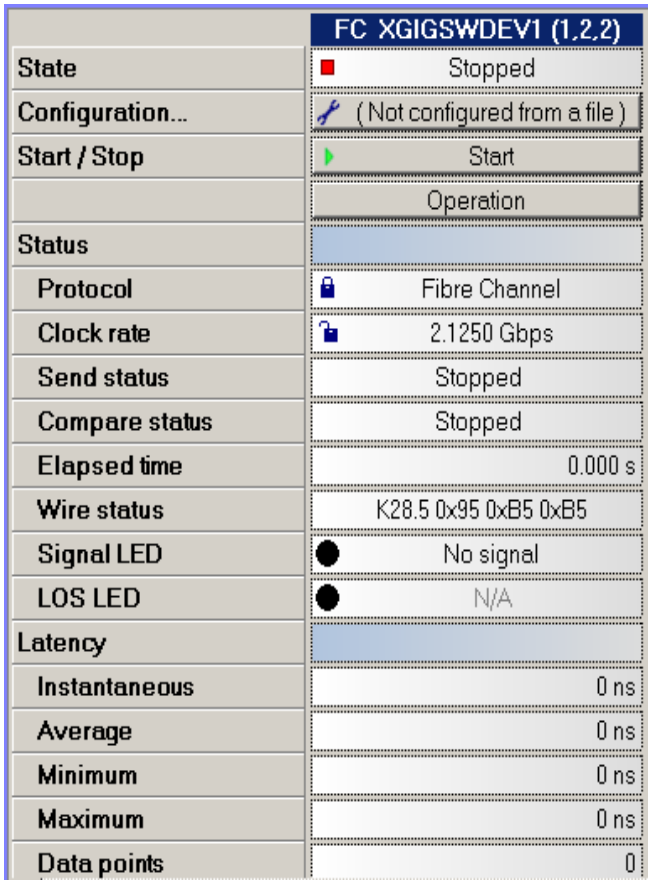
In this chapter:

This chapter describes how to run a Latency measurement and what you can observe while running a test.

After you have configured your latency settings described in Chapter 4, “Configuring Latency Settings,” you can run your test. You do this from the Latency tab on the main window (Figure 51).

The Latency Parameters Status table displays information about the test you are running or the test that has just completed.

Figure 51: Latency Tab



Using the Latency Parameters Status table

Each Latency device is displayed by a column in the Parameters Status table on the Latency tab (Figure 51). At the top of each column is the protocol and the chassis name, followed by the chassis number, the slot number and port number in parenthesis. Below this is a selection indicator. The selected BERT is indicated by a green check mark under Select in the Ports Manager. When you click the **Start** button and run a Latency measurement, the Parameter status table displays a readout for each port that is running a test; the readout is updated several times a second.

The following metrics are available in the Parameters Status table on the Latency tab.

State Category

This category shows the Latency status:

- Disconnected
- Connecting
- Starting
- Synchronizing
- Running
- Stopping
- Stopped

Configuration File Category

Displays the name of the configuration, if any, loaded into the port. Refer to “Loading BERT Configuration Files” on page 42.

Status Category

This category indicates the current physical setup for Latency.

Protocol

Indicates the protocol for a Latency measurement. You choose a protocol in the Port Selection and Domain Setup window when you lock ports. The small lock icon indicates that the protocol cannot be changed at this stage.

Clock rate

Indicates the clock rate. The closed lock icon indicates you cannot currently change the clock rate; the open lock icon indicates you can change the clock rate. The clock rate can be 1.0625 Gbps, 1.2500 Gbps, 1.5000 Gbps, 2.1250 Gbps, 2.5000 Gbps, 3.0000 Gbps, 4.2500 Gbps or 8.5000 Gbps. Both ports in a port pair must always be set to the same clock rate. Therefore, if you have two ports, and one of them is running, the clock rate is locked on both of them.

Setting the Clock Rate

To change the clock rate:

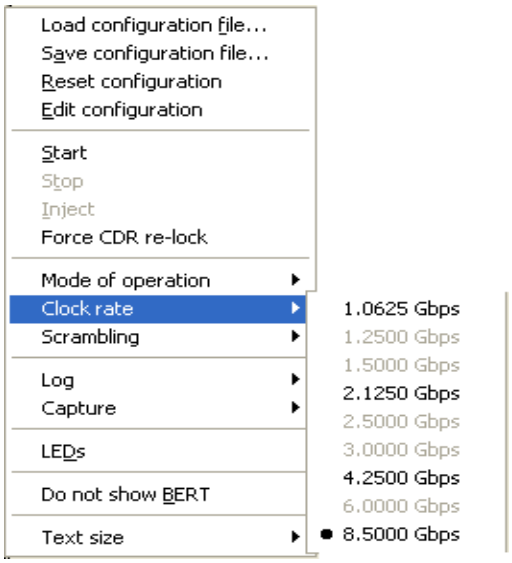
1. Right-click anywhere on the specific port column to open the Parameters context menu (Figure 52).
2. Select **Clock rate**.

   A menu with available choices is displayed
3. Click to choose one.

   Items that are grayed out are not currently available. A bullet is displayed to the left of the currently operating selection.

Note: The clock rate is not saved in the configuration file. This allows Latency configurations to run independently of the clock rate setting and avoids breaking the link to which the device is connected.

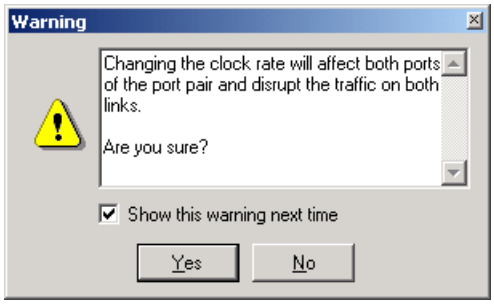
Figure 52: Clock Rate Menu



Note: Two adjacent BERT ports share the same clock rate, specifically ports 1 and 2, and also ports 3 and 4.

Note: Changing the clock rate disrupts the traffic sent from the BERT. A warning message appears when you change the setting (Figure 53).

Figure 53: Changing Clock Rate Warning



Send Status

The Send Status metric reflects the state of transmitting hardware and reports the following activities:

- Stopped
- Sending hardware sync
- Sending...
- Stopping...

Compare Status

The Compare Status metric reflects the state of the compare hardware and reports the following activities:

- Stopped
- Trying to sync up
- Receiving...
- Stopping...

Elapsed Time

The Elapsed Time metric is the time since you clicked **Start** on the Latency Operation bar.

Wire status

Shows the current output of the port.

Signal LED

This LED always shows what is occurring at that moment in a test and therefore changes instantaneously. Table 9 describes the LED colors.

Table 9: Signal LED Descriptions

Port column LED color	Blade LED	Description
Green	Green	Signal is detected and the link is synchronized.
Red	Yellow	Loss of synchronization is occurring.
Black	Off	No signal detected on the link.

LOS LED

The loss of synchronization (LOS) LED shows if loss of synchronization has occurred during the current test (if running) or during the previous test (if stopped). The LED is reset when you start the BERT. The LED colors are described in Table 10.

Table 10: LOS LED Descriptions

Port column LED color	Blade LED	Description
Green	Green	The link is synchronized.
Yellow	Yellow	Loss of synchronization was detected at some point while the test was running.
Red	Blinking Yellow	Loss of synchronization is occurring now or in the last 5 seconds.
Black	Off	Not applicable

Latency Category

The Latency category reports the counter values to the nearest word clock period.

Instantaneous Latency

Reports the most recent latency measurement, or reports “Detecting Errors.”

Average Latency

The average latency computed over the course of the operation.

Minimum Latency

The minimum latency found during the course of the operation.

Maximum Latency

The maximum latency found during the course of the operation.

Data Points

The total number of latency measurements (data frames) utilized for measurement over the course of the operation.

Latency Operation

Latency mode functions similarly in Fibre Channel and Gigabit Ethernet protocols. A simple frame is sent out with zeros in the header fields and a dynamically changing payload. The latency measurement is taken as each frame returns to the device. Note that the latency measurements are only valid for topologies where traffic sent by the device loops, eventually, back to itself. Latency mode does not work when you have two BERTs sending data to each other.

After you select the options you want, click **Start** to begin operation, and click **Stop** to end the measurement. Only the options on the Latency tab apply to this operation; options from the BERT tab do not apply to Latency mode, for example, stop on Loss of Sync.

While running, any frames returning with obvious errors that corrupt the latency measurement are ignored. In the event of Loss of Sync or Loss of Signal, the Instantaneous Latency parameter reports “Detecting Errors.”

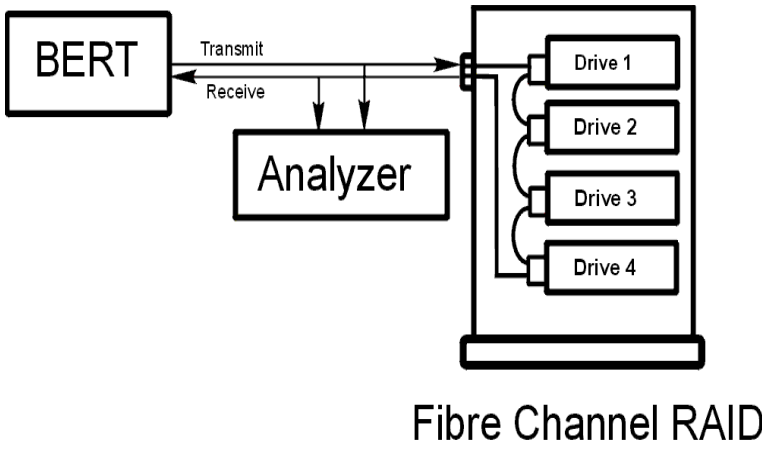
Chapter 6

Bit Error Rate Testing on a Fibre Channel RAID Application Note

In this chapter:

This application note describes how to use the Xgig BERT to test a Fibre Channel RAID (Figure 54).

Figure 54: Using BERT to Test a Fibre Channel RAID



Fibre Channel Physical Layer Testing

Manufacturers and integrators of Fibre Channel (FC) systems and devices need a method of testing the physical integrity of their hardware components before and after these components are assembled into complex systems. Testing ensures that no physical faults that might compromise system performance are introduced into the system during the manufacturing process. Bit Error Rate Testing (BERT) is an effective verification method that is widely used for data communication applications. Due to the characteristics of Arbitrated Loop topologies, however, BERT testing of complex FC systems, such as RAIDs, presents challenges to traditional BERT testers.

The data path components of an FC RAID consist of the input/output transceivers, backplane wiring, port bypass circuits, and the elasticity buffers of the installed drives. A traditional BERT transmits a well known bit stream through the data path and monitors the returning stream for changes in the pattern caused by inverted, inserted, or deleted bits. Bit errors are counted, divided by the number of bits sent, and a Bit Error Rate is calculated. The resulting value is compared to a reference value (typically 10^{-12} for FC systems) to determine if the devices are providing acceptable performance.

The unique characteristics of FC Arbitrated Loops can create errors in the BERT statistics even for properly working systems. Inserting or deleting fill words as the data flows through elasticity buffers will alter the bit stream, resulting in reported errors. Additionally, drive buffers might not pass an arbitrary sequence of bits, but instead require a proper FC format. Finally, the drives comprising the FC RAID will need to select a temporary loop master by performing the Loop Initialization Protocol. The BERT must allow the necessary exchanges to pass through and complete before it begins its own testing; traditional BERTs do not have this capability.

Using the Xgig BERT Fibre Channel System

The Xgig BERT Fibre Channel system has been developed with features that directly address the requirements that have been described.

To test RAID systems you need to:

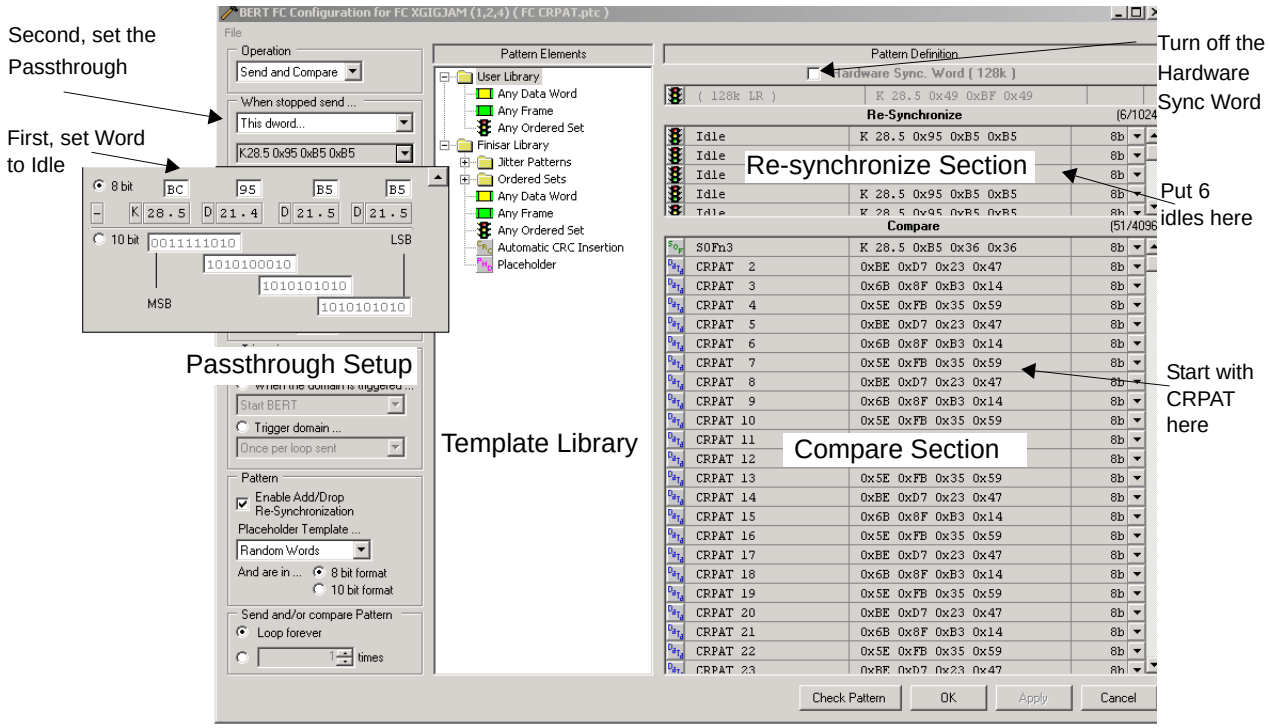
1 Plan the script you are going to use to test the RAID. The script consists of two parts:

- Re-Synchronize —This section of the tool provides the required fill words, such as IDLE, between the frames of the Compare section. Since this portion of the returning stream is not compared, it can contain added or deleted words with no effect on the BERT statistics. The Re-Synchronize feature permits the BERT to accommodate the addition or deletion of fill words by elasticity buffers.
- Compare—Typically constructed as an FC frame (SOF, contents, CRC, EOF), the BERT detects this portion of the returning bit stream and compares the sequence, bit by bit with the original, to detect errors. Any changes in the bit sequence are reported in the BERT statistics. You can select pre-configured FC frames from the Template Library supplied with the system or create your own. You can edit scripts at the 8b or 10b level. This feature allows the BERT to satisfy the requirement of FC formatting the bit stream.

You might want to create your script using the BERT Configuration window. You can choose an FC frame from the Template Library and load it into the Compare section of the Xgig BERT (Figure 55).

Alternatively, you might want to load a sample configuration file such as FC CRPAT.ptc. This single frame contains a bit pattern intended to stress the link; the Re-Synchronization section contains six IDLE words and the Passthrough flush word is set to IDLE.

Figure 55: Xgig BERT Compare Section



2 Make sure the Xgig BERT is set to Passthrough mode before you power up the RAID. Turn off the Hardware Sync Word, then click **Apply**.

3 To perform a BERT on a fully populated RAID, the attached drives must be in an idle state where they will simply pass the data bits around the loop.

To reach this state the drives must log-in with a loop master. In this test, there is no initiator on the loop (the BERT does not participate) and the drive with the lowest worldwide name will be selected as the temporary loop master.

Power up the drives so that they initialize and then begin transmitting IDLE around the loop.

4 Click **Start** on the BERT tab to run the BERT.

The Xgig BERT utilizes the Passthrough mode that allows it to step off of the loop until the initialization process is complete. Once the drives are initialized, the Xgig BERT can then step back on and begin sending its script. In addition, Passthrough mode flushes the loop with one million $(1024)^2$ user-selectable words when the test is stopped. This operation ensures that, if the test is restarted, none of the original frames continue to circulate in the loop. These frames could potentially become truncated by the restart and result in incorrect error reporting by the BERT.

BERT Statistics

When the Xgig BERT application begins reporting the progress of the test, it indicates the total number of bits sent and the total number of bit errors detected (Figure 56). When a sufficient amount of data has been transmitted, you can stop the BERT.

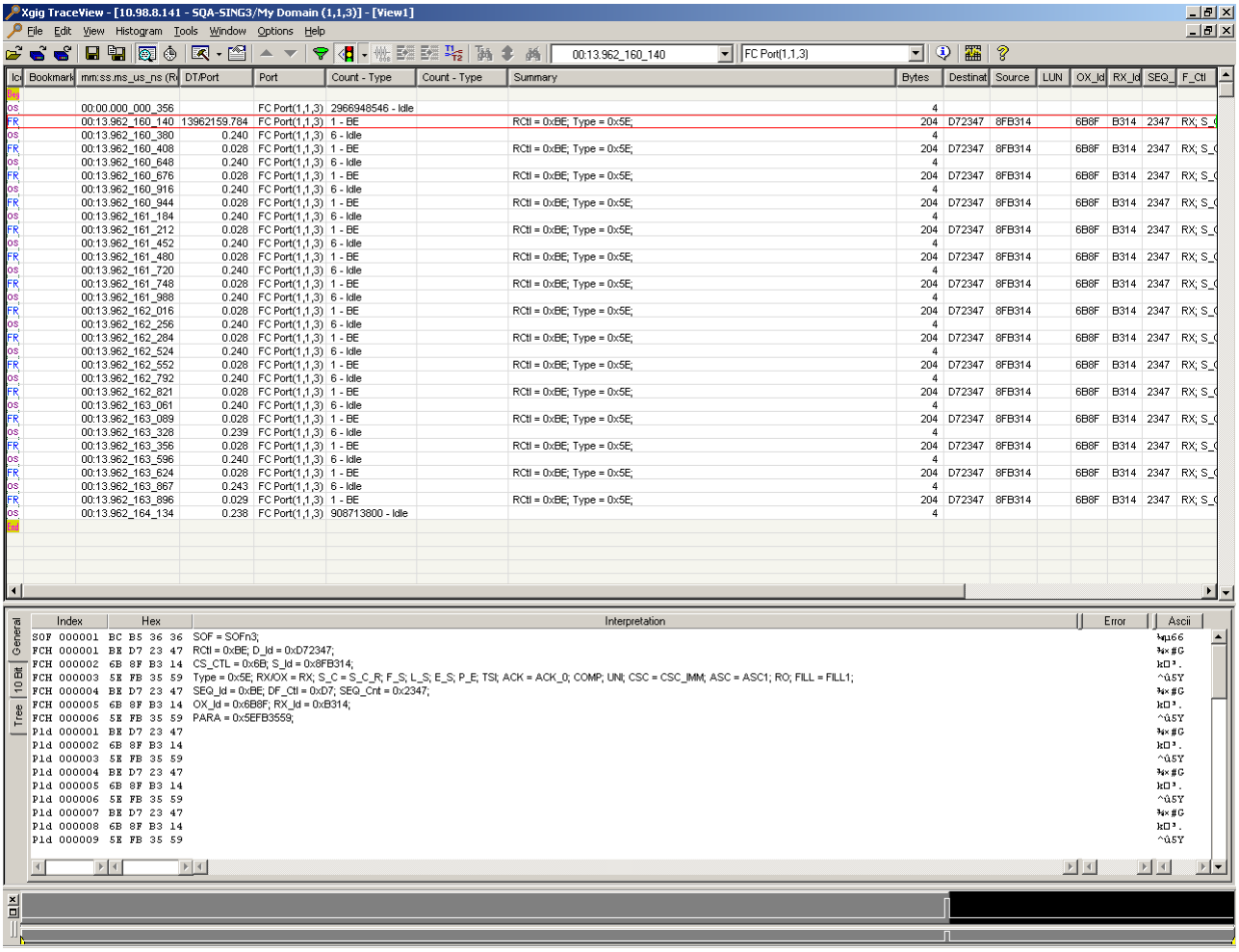
Figure 56: BERT Tab

	FC XGIGSWDEV1 (1,1,1)	FC XGIGSWDEV1 (1,1,3)
State	Stopped	Stopped
Configuration...	FC CJTPAT.ptc	FC CJTPAT.ptc
Start / Stop	Start	Start
	Inject	Inject
	View capture	View capture
	Operation	Operation
Status		
Protocol	Fibre Channel	Fibre Channel
Clock rate	8.5000 Gbps	8.5000 Gbps
Send status	Stopped	Stopped
Compare status	Stopped	Stopped
Elapsed time	311.000 ms	0.000 s
Bit error rate	N/A	N/A
Wire status	K28.5 0x95 0xB5 0xB5	K28.5 0x95 0xB5 0xB5
Signal LED	Signal	Signal
LOS LED	Synchronized	N/A
Mismatches LED	No mismatches	N/A
Log	Log available	No log available
Capture	Capture available	No capture available
Sent		
Bits	2.568 883 680 10^9	0
Bytes	256.888 368 10^6	0
Dual bytes	128.444 184 10^6	0

Trace Capture Example

In this example, the BERT is set to loop on the script 15 times and stop. An Xgig Fibre Channel Analyzer is used to capture a trace of the activity on the loop and the data is displayed in Xgig TraceViewer in Figure 57.

Figure 57: TraceViewer Data



The first and last line of the trace show the IDLEs on the loop before the test begins and after the test is stopped. The remaining lines are 15 repetitions of the CRPAT frame with the 6 IDLEs of the Re-Synchronize section separating the frames. After the fifteenth frame the Xgig BERT flushes the loop with one million IDLEs, which then continue to circulate around the loop until the next test is started.

Chapter 7

Xgig BERT Troubleshooting Tips

The chapter contains some possible problems you might encounter when you are using the Xgig BERT and their solutions.

Symptom:

The receive status won't count compared bits in Send and Compare Mode.

Solution:

Check the following:

- Start word is not an 8b EOF or a Gigabit Ethernet Termination element
- Start word is not the Placeholder or Automatic CRC Insertion element
- Note that the first word must be found without any bit errors
- In Re-Sync Mode, all comma characters are only in the byte 0 (msb) position for Fibre Channel or only byte 0 or byte 2 for Gigabit Ethernet

Symptom:

The Automatic CRC calculator is wrong.

Solution:

Confirm that there are no 10B values between the SOF/SDF Indicator and the Automatic CRC Insertion element. Either an SOF or SDF Indicator and the Automatic CRC Indicator must be present.

Symptom:

Bit errors won't go away with this pattern.

Solution:

Confirm that all pattern elements and Placeholders are 8-bit.

Symptom:

My statistics don't seem quite accurate.

Solution:

Remember that the Start Word in the Compare Zone is not counted in compare statistics during the very first loop in Non-Sync Mode, and is not counted during every loop in Re-Sync Mode. Sending is always stopped after comparing, so that sent statistics are greater than received statistics.

Symptom:

Compare Only mode is not working

Solution:

If the receiver misses the hardware synchronizing section of the pattern, the sender must be stopped and started again.

Symptom:

If I pull the cable and re-insert it, Xgig BERT sometimes compares and sometimes not.

Solution:

The receiver must see the hardware synchronizing section of the pattern to get started. You cannot use placeholders if you intend to remove the cable and re-insert it after the pattern is running. The transmit placeholders will continue while the compare placeholders remain frozen. You must use a re-synchronizing pattern with no placeholder elements.

Symptom:

Re-Timing or Re-Synchronizing does not work correctly.

Solution:

You must have your add/drop words only in the Re-synchronization window. If these words are in the compare section as well, the device under test may add/drop them and the remainder of the compare section will fail to compare well. Make sure Enable Add/Drop Re-Synchronization is checked.

Symptom:

I can’t get a TTL pulse per loop out with this pattern.

Solution:

The trigger out pulse from the port goes to the motherboard and then to the TTL out connector, and is lengthened and retimed in the process. Use a bigger pattern.

Symptom:

I get unexpected disparity errors with this pattern.

Solution:

In general, 8-bit patterns result in proper disparity automatically. In Fibre Channel, 8-bit ordered sets are recognized by hardware and, other than EOF, assume and force a negative running disparity prior to the K28.5. 10-bit values are transmitted without regard to disparity. You must correct 10-bit value errors. In Gigabit Ethernet, I1 Ordered Sets will always be encoded with incoming positive running disparity and I2 will always be encoded with negative.

Symptom:

If you disconnect the SFP or the cable, (the Xgig BERT is no longer receiving a valid signal) the counters stop counting and the display information is no longer valid. Then, if you reconnect the SFP or cable the counters start accumulating, but the values shown do not reflect the errors that occurred during loss of signal.

Solution:

You must restart the BERT to get accurate information. The loss of signal event is displayed with the LOS LED.

Symptom:

The **Start** button is grayed out.

Solution:

You do not have a port selected, or there are no words in the Compare Zone.

Appendix A

Fibre Channel Ordered Sets - Partial List

Fibre Channel defines certain combinations of characters called Ordered Sets. The table in this appendix shows a partial list. The following abbreviations are used in the table:

SOF Start-of-frame delimiter

EOF End-of-frame delimiter

ALPA, D, S, Type Arbitrated Loop Physical Address, Destination, Source, Mark Type. These are limited to 127 specific hex values.

Name	Function	Beginning RD	Ordered Set	8 Bit Hex
SOFc1	SOF Connect Class 1	Negative	K28.5 D21.5 D23.0 D23.0	K28.5 B5 17 17
SOFi1	SOF Initiate Class 1	Negative	K28.5 D21.5 D23.2 D23.2	K28.5 B5 57 57
SOFn1	SOF Normal Class 1	Negative	K28.5 D21.5 D23.1 D23.1	K28.5 B5 37 37
SOFi2	SOF Initiate Class 2	Negative	K28.5 D21.5 D21.2 D21.2	K28.5 B5 55 55
SOFn2	SOF Normal Class 2	Negative	K28.5 D21.5 D21.1 D21.1	K28.5 B5 35 35
SOFi3	SOF Initiate Class 3	Negative	K28.5 D21.5 D22.2 D22.2	K28.5 B5 56 56
SOFn3	SOF Normal Class 3	Negative	K28.5 D21.5 D22.1 D22.1	K28.5 B5 36 36
SOFf	SOF Fabric	Negative	K28.5 D21.5 D24.2 D24.2	K28.5 B5 58 58
SOFc4	SOF Activate Class 4	Negative	K28.5 D21.5 D25.0 D25.0	K28.5 B5 19 19
SOFi4	SOF Initiate Class 4	Negative	K28.5 D21.5 D25.2 D25.2	K28.5 B5 59 59
SOFn4	SOF Normal Class 4	Negative	K28.5 D21.5 D25.1 D25.1	K28.5 B5 39 39

Name	Function	Beginning RD	Ordered Set	8 Bit Hex
EOFt	EOF Terminate	Negative Positive	K28.5 D21.4 D21.3 D21.3 K28.5 D21.5 D21.3 D21.3	K28.5 95 75 75 K28.5 B5 75 75
EOFdt	EOF Disconnect-Terminate	Negative Positive	K28.5 D21.4 D21.4 D21.4 K28.5 D21.5 D21.4 D21.4	K28.5 95 95 95 K28.5 B5 95 95
EOFa	EOF Abort	Negative Positive	K28.5 D21.4 D21.7 D21.7 K28.5 D21.5 D21.7 D21.7	K28.5 95 F5 F5 K28.5 B5 F5 F5
EOFn	EOF Normal	Negative Positive	K28.5 D21.4 D21.6 D21.6 K28.5 D21.5 D21.6 D21.6	K28.5 95 D5 D5 K28.5 B5 D5 D5
EOFdti	EOF Disconnect-Terminate-Invalid	Negative Positive	K28.5 D10.4 D21.4 D21.4 K28.5 D10.5 D21.4 D21.4	K28.5 8A 95 95 K28.5 AA 95 95
EOFni	EOF Normal-Invalid	Negative Positive	K28.5 D10.4 D21.6 D21.6 K28.5 D10.5 D21.6 D21.6	K28.5 8A D5 D5 K28.5 AA D5 D5
EOFrt	EOF Remove-Terminate Class 4	Negative Positive	K28.5 D21.4 D25.4 D25.4 K28.5 D21.5 D25.4 D25.4	K28.5 95 99 99 K28.5 B5 99 99
EOFrti	EOF Remove-Terminate Invalid Class 4	Negative Positive	K28.5 D10.4 D25.4 D25.4 K28.5 D10.5 D25.4 D25.4	K28.5 8A 99 99 K28.5 AA 99 99
IDLE	Idle	Negative	K28.5 D21.4 D21.5 D21.5	K28.5 95 B5 B5
R_RDY	Receiver_Ready	Negative	K28.5 D21.4 D10.2 D10.2	K28.5 95 4A 4A5
VC_RDY	Virtual Circuit Ready	Negative	K28.5 D21.7 VC.ID VC.ID	K28.5 F5 xx xx
BB_SCs	Buffer-to-buffer State Change (SOF)	Negative	K28.5 D21.4 D22.4 D22.4	K28.5 95 96 96
BB_SCr	Buffer-to-buffer State Change (R_RDY)	Negative	K28.5 D21.4 D22.6 D22.6	K28.5 95 D6 D6
SYNx	Clock Synchronization Word x	Negative	K28.5 D31.3 CS_x CS_x	K28.5 7F xx xx
SYNy	Clock Synchronization Word y	Negative	K28.5 D31.3 CS_y CS_y	K28.5 7F xx xx
SYNz	Clock Synchronization Word z	Negative	K28.5 D31.3 CS_z CS_z	K28.5 7F xx xx
OLS	Offline	Negative	K28.5 D21.1 D10.4 D21.2	K28.5 35 8A 55
NOS	Not_Operational	Negative	K28.5 D21.2 D31.5 D5.2	K28.5 55 BF 45
LR	Link_Reset	Negative	K28.5 D9.2 D31.5 D9.2	K28.5 49 BF 49
LRR	Link_Reset_Response	Negative	K28.5 D21.1 D31.5 D9.2	K28.5 55 BF 49
OPNyx	Open Loop Port	Negative	K28.5 D17.4 ALPD ALPS	K28.5 91 xx xx
OPNfr	Open Loop Port	Negative	K28.5 D17.4 D31.7 D31.7	K28.5 91 FF FF
CLS	Close Loop Port	Negative	K28.5 D5.4 D21.5 D21.5	K28.5 85 B5 B5
MRK	Mark	Negative	K28.5 D31.2 type ALPS	K28.5 5F xx xx
LIP	Loop Initialization, Acquire PA	Negative	K28.5 D21.0 D23.7 D23.7	K28.5 15 F7 F7
LIP	Loop Initialization, Rcvr Fail	Negative	K28.5 D21.0 D24.7 D23.7	K28.5 15 F8 F7
LIP	Loop Initialization, Reinitialize	Negative	K28.5 D21.0 D23.7 ALPS	K28.5 15 F7 xx
LIP	Loop Initialization, Fail at PS	Negative	K28.5 D21.0 D24.7 ALPS	K28.5 15 F8 xx
LIP	Loop Initialization, Reset PD	Negative	K28.5 D21.0 ALPD ALPS	K28.5 15 xx xx
LPEyx	Loop Port Enable, enable PD	Negative	K28.5 D5.0 ALPD ALPS	K28.5 05 xx xx
LPEfx	Loop Port Enable, enable all	Negative	K28.5 D5.0 D31.7 ALPS	K28.5 05 FF xx
LPByx	Loop Port Bypass, bypass PD	Negative	K28.5 D9.0 ALPD ALPS	K28.5 09 xx xx
ARBx	Arbitrate For Loop	Negative	K28.5 D20.4 ALPS ALPS	K28.5 94 xx xx
ARB(F0)	Arbitrate For Loop, fairness	Negative	K28.5 D20.4 D16.7 D16.7	K28.5 94 F0 F0

Appendix B

8-Bit/10-Bit Mapping

This appendix contains tables sorted by values for 8-bit/10-bit mapping.

The following table lists:

Legal 8-Bit/10-Bit Characters Sorted by 10-Bit Value

10B Dec	8B Dec	ASCII+	HEX	Previous Disparity	Data Byte Name	10 B	Comment
85	87	W	57	RD +	D23.2	00 0101 0101	
86	215	×	D7	RD +	D23.6	00 0101 0110	
87	247	÷	F7	RD +	K23.7	00 0101 0111	
89	55	7	37	RD +	D23.1	00 0101 1001	
90	183	·	B7	RD +	D23.5	00 0101 1010	
91	23	ETB	17	RD +	D23.0	00 0101 1011	
92	119	w	77	RD +	D23.3	00 0101 1100	
93	151	—	97	RD +	D23.4	00 0101 1101	
94	247	÷	F7	RD +	D23.7	00 0101 1110	
101	72	H	48	RD +	D8.2	00 0110 0101	
102	200	È	C8	RD +	D8.6	00 0110 0110	
105	40	(	28	RD +	D8.1	00 0110 1001	
106	168	¨	A8	RD +	D8.5	00 0110 1010	
107	8	BS	08	RD +	D8.0	00 0110 1011	
108	104	h	68	RD +	D8.3	00 0110 1100	
109	136	ˆ	88	RD +	D8.4	00 0110 1101	
110	232	è	E8	RD +	D8.7	00 0110 1110	
113	231	ç	E7	RD +	D7.7	00 0111 0001	
114	135	‡	87	RD +	D7.4	00 0111 0010	
115	103	g	67	RD +	D7.3	00 0111 0011	
116	7	BEL	07	RD +	D7.0	00 0111 0100	
117	71	G	47	RD +	D7.2	00 0111 0101	
118	199	Ç	C7	RD +	D7.6	00 0111 0110	
121	39	'	27	RD +	D7.1	00 0111 1001	
122	167	§	A7	RD +	D7.5	00 0111 1010	
149	91	[	5B	RD +	D27.2	00 1001 0101	
150	219	Û	DB	RD +	D27.6	00 1001 0110	
151	251	û	FB	RD +	K27.7	00 1001 0111	
153	59	;	3B	RD +	D27.1	00 1001 1001	
154	187	»	BB	RD +	D27.5	00 1001 1010	
155	27	ESC	1B	RD +	D27.0	00 1001 1011	
156	123	{	7B	RD +	D27.3	00 1001 1100	
157	155	›	9B	RD +	D27.4	00 1001 1101	
158	251	û	FB	RD +	D27.7	00 1001 1110	
165	68	D	44	RD +	D4.2	00 1010 0101	
166	196	Ä	C4	RD +	D4.6	00 1010 0110	
169	36	$	24	RD +	D4.1	00 1010 1001	
170	164	¤	A4	RD +	D4.5	00 1010 1010	
171	4	EOT	04	RD +	D4.0	00 1010 1011	
172	100	d	64	RD +	D4.3	00 1010 1100	
173	132	„	84	RD +	D4.4	00 1010 1101	
174	228	ä	E4	RD +	D4.7	00 1010 1110	
177	244	ô	F4	RD +	D20.7	00 1011 0001	
178	148	”	94	RD +	D20.4	00 1011 0010	
179	116	t	74	RD +	D20.3	00 1011 0011	
180	20	DC4	14	RD +	D20.0	00 1011 0100	
181	84	T	54	RD+/--	D20.2	00 1011 0101	
182	212	Ô	D4	RD+/--	D20.6	00 1011 0110	
183	244	ô	F4	RD--	D20.7	00 1011 0111	
185	52	4	34	RD+/--	D20.1	00 1011 1001	
186	180	´	B4	RD+/--	D20.5	00 1011 1010	
187	20	DC4	14	RD--	D20.0	00 1011 1011	
188	116	t	74	RD--	D20.3	00 1011 1100	
189	148	”	94	RD--	D20.4	00 1011 1101	
197	88	X	58	RD +	D24.2	00 1100 0101	
198	216	Ø	D8	RD +	D24.6	00 1100 0110	
201	56	8	38	RD +	D24.1	00 1100 1001	
202	184	¸	B8	RD +	D24.5	00 1100 1010	
203	24	CAN	18	RD +	D24.0	00 1100 1011	
204	120	x	78	RD +	D24.3	00 1100 1100	
205	152	˜	98	RD +	D24.4	00 1100 1101	
206	248	ø	F8	RD +	D24.7	00 1100 1110	
209	236	ì	EC	RD +	D12.7	00 1101 0001	
210	140	Œ	8C	RD +	D12.4	00 1101 0010	
211	108	l	6C	RD +	D12.3	00 1101 0011	
212	12	FF	0C	RD +	D12.0	00 1101 0100	
213	76	L	4C	RD+/--	D12.2	00 1101 0101	
214	204	Ì	CC	RD+/--	D12.6	00 1101 0110	
217	44	,	2C	RD+/--	D12.1	00 1101 1001	
218	172	¬	AC	RD+/--	D12.5	00 1101 1010	
219	12	FF	0C	RD--	D12.0	00 1101 1011	
220	108	l	6C	RD--	D12.3	00 1101 1100	
221	140	Œ	8C	RD--	D12.4	00 1101 1101	
222	236	ì	EC	RD--	D12.7	00 1101 1110	
225	252	ü	FC	RD +	D28.7	00 1110 0001	
226	156	œ	9C	RD +	D28.4	00 1110 0010	
227	124	|	7C	RD +	D28.3	00 1110 0011	
228	28	FS	1C	RD +	D28.0	00 1110 0100	
229	92	\	5C	RD+/--	D28.2	00 1110 0101	
230	220	Ü	DC	RD+/--	D28.6	00 1110 0110	
233	60	<	3C	RD+/--	D28.1	00 1110 1001	
234	188	¼	BC	RD+/--	D28.5	00 1110 1010	
235	28	FS	1C	RD--	D28.0	00 1110 1011	
236	124	|	7C	RD--	D28.3	00 1110 1100	
237	156	œ	9C	RD--	D28.4	00 1110 1101	
238	252	ü	FC	RD--	D28.7	00 1110 1110	
242	156	œ	9C	RD --	K28.4	00 1111 0010	Reserved*
243	124	|	7C	RD --	K28.3	00 1111 0011	Reserved*
244	28	FS	1C	RD --	K28.0	00 1111 0100	Reserved*
245	92	\	5C	RD --	K28.2	00 1111 0101	Reserved*
246	220	Ü	DC	RD --	K28.6	00 1111 0110	Reserved*
248	252	ü	FC	RD --	K28.7	00 1111 1000	Test
249	60	<	3C	RD --	K28.1	00 1111 1001	Reserved*
250	188	¼	BC	RD --	K28.5	00 1111 1010	Sync
277	93	]	5D	RD +	D29.2	01 0001 0101	
278	221	Ý	DD	RD +	D29.6	01 0001 0110	
279	253	ý	FD	RD +	K29.7	01 0001 0111	
281	61	=	3D	RD +	D29.1	01 0001 1001	
282	189	½	BD	RD +	D29.5	01 0001 1010	
283	29	GS	1D	RD +	D29.0	01 0001 1011	
284	125	}	7D	RD +	D29.3	01 0001 1100	
285	157	_	9D	RD +	D29.4	01 0001 1101	
286	253	ý	FD	RD +	D29.7	01 0001 1110	
293	66	B	42	RD +	D2.2	01 0010 0101	
294	194	Â	C2	RD +	D2.6	01 0010 0110	
297	34	"	22	RD +	D2.1	01 0010 1001	
298	162	¢	A2	RD +	D2.5	01 0010 1010	
299	2	STX	02	RD +	D2.0	01 0010 1011	
300	98	b	62	RD +	D2.3	01 0010 1100	
301	130	‚	82	RD +	D2.4	01 0010 1101	
302	226	â	E2	RD +	D2.7	01 0010 1110	
305	242	ò	F2	RD +	D18.7	01 0011 0001	
306	146	’	92	RD +	D18.4	01 0011 0010	
307	114	r	72	RD +	D18.3	01 0011 0011	
308	18	DC2	12	RD +	D18.0	01 0011 0100	
309	82	R	52	RD+/--	D18.2	01 0011 0101	
310	210	Ò	D2	RD+/--	D18.6	01 0011 0110	
311	242	ò	F2	RD--	D18.7	01 0011 0111	
313	50	2	32	RD+/--	D18.1	01 0011 1001	
314	178	²	B2	RD+/--	D18.5	01 0011 1010	
315	18	DC2	12	RD--	D18.0	01 0011 1011	
316	114	r	72	RD--	D18.3	01 0011 1100	
317	146	’	92	RD--	D18.4	01 0011 1101	
325	95	_	5F	RD +	D31.2	01 0100 0101	
326	223	ß	DF	RD +	D31.6	01 0100 0110	
329	63	?	3F	RD +	D31.1	01 0100 1001	
330	191	¿	BF	RD +	D31.5	01 0100 1010	
331	31	US	1F	RD +	D31.0	01 0100 1011	
332	127	DELETE	7F	RD +	D31.3	01 0100 1100	
333	159	Ÿ	9F	RD +	D31.4	01 0100 1101	
334	255	ÿ	FF	RD +	D31.7	01 0100 1110	

337	234	ê	EA	RD +	D10.7	01 0101 0001
338	138	Š	8A	RD +	D10.4	01 0101 0010
339	106	j	6A	RD +	D10.3	01 0101 0011
340	10	LF	0A	RD +	D10.0	01 0101 0100
341	74	J	4A	RD+/--	D10.2	01 0101 0101
342	202	Ê	CA	RD+/--	D10.6	01 0101 0110
345	42	*	2A	RD+/--	D10.1	01 0101 1001
346	170	ª	AA	RD+/--	D10.5	01 0101 1010
347	10	LF	0A	RD--	D10.0	01 0101 1011
348	106	j	6A	RD--	D10.3	01 0101 1100
349	138	Š	8A	RD--	D10.4	01 0101 1101
350	234	ê	EA	RD--	D10.7	01 0101 1110
353	250	ú	FA	RD +	D26.7	01 0110 0001
354	154	š	9A	RD +	D26.4	01 0110 0010
355	122	z	7A	RD +	D26.3	01 0110 0011
356	26	SUB	1A	RD +	D26.0	01 0110 0100
357	90	Z	5A	RD+/--	D26.2	01 0110 0101
358	218	Ú	DA	RD+/--	D26.6	01 0110 0110
361	58	:	3A	RD+/--	D26.1	01 0110 1001
362	186	º	BA	RD+/--	D26.5	01 0110 1010
363	26	SUB	1A	RD--	D26.0	01 0110 1011
364	122	z	7A	RD--	D26.3	01 0110 1100
365	154	š	9A	RD--	D26.4	01 0110 1101
366	250	ú	FA	RD--	D26.7	01 0110 1110
369	239	ï	EF	RD--	D15.7	01 0111 0001
370	143	_	8F	RD--	D15.4	01 0111 0010
371	111	o	6F	RD--	D15.3	01 0111 0011
372	15	SI	0F	RD--	D15.0	01 0111 0100
373	79	O	4F	RD--	D15.2	01 0111 0101
374	207	Ï	CF	RD--	D15.6	01 0111 0110
377	47	/	2F	RD--	D15.1	01 0111 1001
378	175	¯	AF	RD--	D15.5	01 0111 1010
389	64	@	40	RD +	D0.2	01 1000 0101
390	192	À	C0	RD +	D0.6	01 1000 0110
393	32	SPACE	20	RD +	D0.1	01 1000 1001
394	160		A0	RD +	D0.5	01 1000 1010
395	0	NUL	00	RD +	D0.0	01 1000 1011
396	96	`	60	RD +	D0.3	01 1000 1100
397	128	_	80	RD +	D0.4	01 1000 1101
398	224	à	E0	RD +	D0.7	01 1000 1110
401	230	æ	E6	RD +	D6.7	01 1001 0001
402	134	†	86	RD +	D6.4	01 1001 0010
403	102	f	66	RD +	D6.3	01 1001 0011
404	6	ACK	06	RD +	D6.0	01 1001 0100
405	70	F	46	RD+/--	D6.2	01 1001 0101
406	198	Æ	C6	RD+/--	D6.6	01 1001 0110
409	38	&	26	RD+/--	D6.1	01 1001 1001
410	166	¦	A6	RD+/--	D6.5	01 1001 1010
411	6	ACK	06	RD--	D6.0	01 1001 1011
412	102	f	66	RD--	D6.3	01 1001 1100
413	134	†	86	RD--	D6.4	01 1001 1101
414	230	æ	E6	RD--	D6.7	01 1001 1110
417	246	ö	F6	RD +	D22.7	01 1010 0001
418	150	–	96	RD +	D22.4	01 1010 0010
419	118	v	76	RD +	D22.3	01 1010 0011
420	22	SYN	16	RD +	D22.0	01 1010 0100
421	86	V	56	RD+/--	D22.2	01 1010 0101
422	214	Ö	D6	RD+/--	D22.6	01 1010 0110
425	54	6	36	RD+/--	D22.1	01 1010 1001
426	182	¶	B6	RD+/--	D22.5	01 1010 1010
427	22	SYN	16	RD--	D22.0	01 1010 1011
428	118	v	76	RD--	D22.3	01 1010 1100
429	150	–	96	RD--	D22.4	01 1010 1101
430	246	ö	F6	RD--	D22.7	01 1010 1110
433	240	ð	F0	RD--	D16.7	01 1011 0001
434	144	_	90	RD--	D16.4	01 1011 0010
435	112	p	70	RD--	D16.3	01 1011 0011
436	16	DLE	10	RD--	D16.0	01 1011 0100
437	80	P	50	RD--	D16.2	01 1011 0101
438	208	Ð	D0	RD--	D16.6	01 1011 0110
441	48	0	30	RD--	D16.1	01 1011 1001
442	176	°	B0	RD--	D16.5	01 1011 1010
450	142	_	8E	RD +	D14.4	01 1100 0010
451	110	n	6E	RD +	D14.3	01 1100 0011
452	14	SO	0E	RD +	D14.0	01 1100 0100
453	78	N	4E	RD+/--	D14.2	01 1100 0101
454	206	Î	CE	RD+/--	D14.6	01 1100 0110
456	238	î	EE	RD +	D14.7	01 1100 1000
457	46	.	2E	RD+/--	D14.1	01 1100 1001
458	174	®	AE	RD+/--	D14.5	01 1100 1010
459	14	SO	0E	RD--	D14.0	01 1100 1011
460	110	n	6E	RD--	D14.3	01 1100 1100
461	142	_	8E	RD--	D14.4	01 1100 1101
462	238	Î	EE	RD--	D14.7	01 1100 1110
465	225	á	E1	RD--	D1.7	01 1101 0001
466	129	_	81	RD--	D1.4	01 1101 0010
467	97	a	61	RD--	D1.3	01 1101 0011
468	1	SOH	01	RD--	D1.0	01 1101 0100
469	65	A	41	RD--	D1.2	01 1101 0101
470	193	Á	C1	RD--	D1.6	01 1101 0110
473	33	!	21	RD--	D1.1	01 1101 1001
474	161	¡	A1	RD--	D1.5	01 1101 1010
481	254	þ	FE	RD--	D30.7	01 1110 0001
482	158	_	9E	RD--	D30.4	01 1110 0010
483	126	~	7E	RD--	D30.3	01 1110 0011
484	30	RS	1E	RD--	D30.0	01 1110 0100
485	94	^	5E	RD--	D30.2	01 1110 0101
486	222	Þ	DE	RD--	D30.6	01 1110 0110
488	254	þ	FE	RD --	K30.7	01 1110 1000 Reserved*
489	62	>	3E	RD--	D30.1	01 1110 1001
490	190	¾	BE	RD--	D30.5	01 1110 1010
533	94	^	5E	RD +	D30.2	10 0001 0101
534	222	Þ	DE	RD +	D30.6	10 0001 0110
535	254	þ	FE	RD +	K30.7	10 0001 0111
537	62	>	3E	RD +	D30.1	10 0001 1001
538	190	¾	BE	RD +	D30.5	10 0001 1010
539	30	RS	1E	RD +	D30.0	10 0001 1011
540	126	~	7E	RD +	D30.3	10 0001 1100
541	158	_	9E	RD +	D30.4	10 0001 1101
542	254	þ	FE	RD +	D30.7	10 0001 1110
549	65	A	41	RD +	D1.2	10 0010 0101
550	193	Á	C1	RD +	D1.6	10 0010 0110
553	33	!	21	RD +	D1.1	10 0010 1001
554	161	¡	A1	RD +	D1.5	10 0010 1010
555	1	SOH	01	RD +	D1.0	10 0010 1011
556	97	a	61	RD +	D1.3	10 0010 1100
557	129	_	81	RD +	D1.4	10 0010 1101
558	225	á	E1	RD +	D1.7	10 0010 1110
561	241	ñ	F1	RD +	D17.7	10 0011 0001
562	145	‘	91	RD +	D17.4	10 0011 0010
563	113	q	71	RD +	D17.3	10 0011 0011
564	17	DC1	11	RD +	D17.0	10 0011 0100
565	81	Q	51	RD+/--	D17.2	10 0011 0101
566	209	Ñ	D1	RD+/--	D17.6	10 0011 0110
567	241	ñ	F1	RD--	D17.7	10 0011 0111
569	49	1	31	RD+/--	D17.1	10 0011 1001
570	177	±	B1	RD+/--	D17.5	10 0011 1010
571	17	DC1	11	RD--	D17.0	10 0011 1011
572	113	q	71	RD--	D17.3	10 0011 1100
573	145	‘	91	RD--	D17.4	10 0011 1101
581	80	P	50	RD +	D16.2	10 0100 0101
582	208	Ð	D0	RD +	D16.6	10 0100 0110
585	48	0	30	RD +	D16.1	10 0100 1001
586	176	°	B0	RD +	D16.5	10 0100 1010
587	16	DLE	10	RD +	D16.0	10 0100 1011
588	112	p	70	RD +	D16.3	10 0100 1100
589	144	_	90	RD +	D16.4	10 0100 1101
590	240	ð	F0	RD +	D16.7	10 0100 1110
593	233	é	E9	RD +	D9.7	10 0101 0001
594	137	‰	89	RD +	D9.4	10 0101 0010
595	105	i	69	RD +	D9.3	10 0101 0011
596	9	HT	09	RD +	D9.0	10 0101 0100
597	73	I	49	RD+/--	D9.2	10 0101 0101
598	201	É	C9	RD+/--	D9.6	10 0101 0110

601	41	)	29	RD+/--	D9.1	10 0101 1001
602	169	©	A9	RD+/--	D9.5	10 0101 1010
603	9	HT	09	RD--	D9.0	10 0101 1011
604	105	i	69	RD--	D9.3	10 0101 1100
605	137	‰	89	RD--	D9.4	10 0101 1101
606	233	é	E9	RD--	D9.7	10 0101 1110
609	249	ù	F9	RD +	D25.7	10 0110 0001
610	153	™	99	RD +	D25.4	10 0110 0010
611	121	y	79	RD +	D25.3	10 0110 0011
612	25	EM	19	RD +	D25.0	10 0110 0100
613	89	Y	59	RD+/--	D25.2	10 0110 0101
614	217	Ù	D9	RD+/--	D25.6	10 0110 0110
617	57	9	39	RD+/--	D25.1	10 0110 1001
618	185	¹	B9	RD+/--	D25.5	10 0110 1010
619	25	EM	19	RD--	D25.0	10 0110 1011
620	121	y	79	RD--	D25.3	10 0110 1100
621	153	™	99	RD--	D25.4	10 0110 1101
622	249	ù	F9	RD--	D25.7	10 0110 1110
625	224	à	E0	RD--	D0.7	10 0111 0001
626	128	_	80	RD--	D0.4	10 0111 0010
627	96	`	60	RD--	D0.3	10 0111 0011
628	0	NUL	00	RD--	D0.0	10 0111 0100
629	64	@	40	RD--	D0.2	10 0111 0101
630	192	À	C0	RD--	D0.6	10 0111 0110
633	32	SPACE	20	RD--	D0.1	10 0111 1001
634	160		A0	RD--	D0.5	10 0111 1010
645	79	O	4F	RD +	D15.2	10 1000 0101
646	207	Ï	CF	RD +	D15.6	10 1000 0110
649	47	/	2F	RD +	D15.1	10 1000 1001
650	175	¯	AF	RD +	D15.5	10 1000 1010
651	15	SI	0F	RD +	D15.0	10 1000 1011
652	111	o	6F	RD +	D15.3	10 1000 1100
653	143	_	8F	RD +	D15.4	10 1000 1101
654	239	ï	EF	RD +	D15.7	10 1000 1110
657	229	å	E5	RD +	D5.7	10 1001 0001
658	133	…	85	RD +	D5.4	10 1001 0010
659	101	e	65	RD +	D5.3	10 1001 0011
660	5	ENQ	05	RD +	D5.0	10 1001 0100
661	69	E	45	RD+/--	D5.2	10 1001 0101
662	197	Å	C5	RD+/--	D5.6	10 1001 0110
665	37	%	25	RD+/--	D5.1	10 1001 1001
666	165	¥	A5	RD+/--	D5.5	10 1001 1010
667	5	ENQ	05	RD--	D5.0	10 1001 1011
668	101	e	65	RD--	D5.3	10 1001 1100
669	133	…	85	RD--	D5.4	10 1001 1101
670	229	å	E5	RD--	D5.7	10 1001 1110
673	245	õ	F5	RD +	D21.7	10 1010 0001
674	149	•	95	RD +	D21.4	10 1010 0010
675	117	u	75	RD +	D21.3	10 1010 0011
676	21	NAK	15	RD +	D21.0	10 1010 0100
677	85	U	55	RD+/--	D21.2	10 1010 0101
678	213	Õ	D5	RD+/--	D21.6	10 1010 0110
681	53	5	35	RD+/--	D21.1	10 1010 1001
682	181	µ	B5	RD+/--	D21.5	10 1010 1010
683	21	NAK	15	RD--	D21.0	10 1010 1011
684	117	u	75	RD--	D21.3	10 1010 1100
685	149	•	95	RD--	D21.4	10 1010 1101
686	245	õ	F5	RD--	D21.7	10 1010 1110
689	255	ÿ	FF	RD--	D31.7	10 1011 0001
690	159	Ÿ	9F	RD--	D31.4	10 1011 0010
691	127	DELETE	7F	RD--	D31.3	10 1011 0011
692	31	US	1F	RD--	D31.0	10 1011 0100
693	95	_	5F	RD--	D31.2	10 1011 0101
694	223	ß	DF	RD--	D31.6	10 1011 0110
697	63	?	3F	RD--	D31.1	10 1011 1001
698	191	¿	BF	RD--	D31.5	10 1011 1010
706	141	_	8D	RD +	D13.4	10 1100 0010
707	109	m	6D	RD +	D13.3	10 1100 0011
708	13	CR	0D	RD +	D13.0	10 1100 0100
709	77	M	4D	RD+/--	D13.2	10 1100 0101
710	205	Í	CD	RD+/--	D13.6	10 1100 0110
712	237	í	ED	RD +	D13.7	10 1100 1000
713	45	-	2D	RD+/--	D13.1	10 1100 1001
714	173	-	AD	RD+/--	D13.5	10 1100 1010
715	13	CR	0D	RD--	D13.0	10 1100 1011
716	109	m	6D	RD--	D13.3	10 1100 1100
717	141	_	8D	RD--	D13.4	10 1100 1101
718	237	í	ED	RD--	D13.7	10 1100 1110
721	226	â	E2	RD--	D2.7	10 1101 0001
722	130	‚	82	RD--	D2.4	10 1101 0010
723	98	b	62	RD--	D2.3	10 1101 0011
724	2	STX	02	RD--	D2.0	10 1101 0100
725	66	B	42	RD--	D2.2	10 1101 0101
726	194	Â	C2	RD--	D2.6	10 1101 0110
729	34	"	22	RD--	D2.1	10 1101 1001
730	162	¢	A2	RD--	D2.5	10 1101 1010
737	253	ý	FD	RD--	D29.7	10 1110 0001
738	157	_	9D	RD--	D29.4	10 1110 0010
739	125	}	7D	RD--	D29.3	10 1110 0011
740	29	GS	1D	RD--	D29.0	10 1110 0100
741	93	]	5D	RD--	D29.2	10 1110 0101
742	221	Ý	DD	RD--	D29.6	10 1110 0110
744	253	ý	FD	RD --	K29.7	10 1110 1000 Reserved*
745	61	=	3D	RD--	D29.1	10 1110 1001
746	189	½	BD	RD--	D29.5	10 1110 1010
773	188	¼	BC	RD +	K28.5	11 0000 0101 (Not Used)
774	60	<	3C	RD +	K28.1	11 0000 0110
775	252	ü	FC	RD +	K28.7	11 0000 0111
777	220	Ü	DC	RD +	K28.6	11 0000 1001
778	92	\	5C	RD +	K28.2	11 0000 1010
779	28	FS	1C	RD +	K28.0	11 0000 1011
780	124	|	7C	RD +	K28.3	11 0000 1100
781	156	œ	9C	RD +	K28.4	11 0000 1101
785	227	ã	E3	RD +	D3.7	11 0001 0001
786	131	ƒ	83	RD +	D3.4	11 0001 0010
787	99	c	63	RD +	D3.3	11 0001 0011
788	3	ETX	03	RD +	D3.0	11 0001 0100
789	67	C	43	RD+/--	D3.2	11 0001 0101
790	195	Ã	C3	RD+/--	D3.6	11 0001 0110
793	35	#	23	RD+/--	D3.1	11 0001 1001
794	163	£	A3	RD+/--	D3.5	11 0001 1010
795	3	ETX	03	RD--	D3.0	11 0001 1011
796	99	c	63	RD--	D3.3	11 0001 1100
797	131	ƒ	83	RD--	D3.4	11 0001 1101
798	227	ã	E3	RD--	D3.7	11 0001 1110
801	243	ó	F3	RD +	D19.7	11 0010 0001
802	147	“	93	RD +	D19.4	11 0010 0010
803	115	s	73	RD +	D19.3	11 0010 0011
804	19	DC3	13	RD +	D19.0	11 0010 0100
805	83	S	53	RD+/--	D19.2	11 0010 0101
806	211	Ó	D3	RD+/--	D19.6	11 0010 0110
809	51	3	33	RD+/--	D19.1	11 0010 1001
810	179	³	B3	RD+/--	D19.5	11 0010 1010
811	19	DC3	13	RD--	D19.0	11 0010 1011
812	115	s	73	RD--	D19.3	11 0010 1100
813	147	“	93	RD--	D19.4	11 0010 1101
814	243	ó	F3	RD--	D19.7	11 0010 1110
817	248	ø	F8	RD--	D24.7	11 0011 0001
818	152	˜	98	RD--	D24.4	11 0011 0010
819	120	x	78	RD--	D24.3	11 0011 0011
820	24	CAN	18	RD--	D24.0	11 0011 0100
821	88	X	58	RD--	D24.2	11 0011 0101
822	216	Ø	D8	RD--	D24.6	11 0011 0110
825	56	8	38	RD--	D24.1	11 0011 1001
826	184	¸	B8	RD--	D24.5	11 0011 1010
834	139	‹	8B	RD +	D11.4	11 0100 0010
835	107	k	6B	RD +	D11.3	11 0100 0011
836	11	VT	0B	RD +	D11.0	11 0100 0100
837	75	K	4B	RD+/--	D11.2	11 0100 0101
838	203	Ë	CB	RD+/--	D11.6	11 0100 0110
840	235	ë	EB	RD +	D11.7	11 0100 1000
841	43	+	2B	RD+/--	D11.1	11 0100 1001
842	171	«	AB	RD+/--	D11.5	11 0100 1010
843	11	VT	0B	RD--	D11.0	11 0100 1011

844	107	k	6B	RD--	D11.3	11 0100 1100	
845	139	‹	8B	RD--	D11.4	11 0100 1101	
846	235	ë	EB	RD--	D11.7	11 0100 1110	
849	228	ä	E4	RD--	D4.7	11 0101 0001	
850	132	„	84	RD--	D4.4	11 0101 0010	
851	100	d	64	RD--	D4.3	11 0101 0011	
852	4	EOT	04	RD--	D4.0	11 0101 0100	
853	68	D	44	RD--	D4.2	11 0101 0101	
854	196	Ä	C4	RD--	D4.6	11 0101 0110	
857	36	$	24	RD--	D4.1	11 0101 1001	
858	164	¤	A4	RD--	D4.5	11 0101 1010	
865	251	û	FB	RD--	D27.7	11 0110 0001	
866	155	›	9B	RD--	D27.4	11 0110 0010	
867	123	{	7B	RD--	D27.3	11 0110 0011	
868	27	ESC	1B	RD--	D27.0	11 0110 0100	
869	91	[	5B	RD--	D27.2	11 0110 0101	
870	219	Û	DB	RD--	D27.6	11 0110 0110	
872	251	û	FB	RD --	K27.7	11 0110 1000	Reserved*
873	59	;	3B	RD--	D27.1	11 0110 1001	
874	187	»	BB	RD--	D27.5	11 0110 1010	
901	71	G	47	RD--	D7.2	11 1000 0101	
902	199	Ç	C7	RD--	D7.6	11 1000 0110	
905	39	'	27	RD--	D7.1	11 1000 1001	
906	167	§	A7	RD--	D7.5	11 1000 1010	
907	7	BEL	07	RD--	D7.0	11 1000 1011	
908	103	g	67	RD--	D7.3	11 1000 1100	
909	135	‡	87	RD--	D7.4	11 1000 1101	
910	231	ç	E7	RD--	D7.7	11 1000 1110	
913	232	è	E8	RD--	D8.7	11 1001 0001	
914	136	ˆ	88	RD--	D8.4	11 1001 0010	
915	104	h	68	RD--	D8.3	11 1001 0011	
916	8	BS	08	RD--	D8.0	11 1001 0100	
917	72	H	48	RD--	D8.2	11 1001 0101	
918	200	È	C8	RD--	D8.6	11 1001 0110	
921	40	(	28	RD--	D8.1	11 1001 1001	
922	168	¨	A8	RD--	D8.5	11 1001 1010	
929	247	÷	F7	RD--	D23.7	11 1010 0001	
930	151	—	97	RD--	D23.4	11 1010 0010	
931	119	w	77	RD--	D23.3	11 1010 0011	
932	23	ETB	17	RD--	D23.0	11 1010 0100	
933	87	W	57	RD--	D23.2	11 1010 0101	
934	215	×	D7	RD--	D23.6	11 1010 0110	
936	247	÷	F7	RD --	K23.7	11 1010 1000	Reserved*
937	55	7	37	RD--	D23.1	11 1010 1001	
938	183	·	B7	RD--	D23.5	11 1010 1010	

The following table lists:

10-Bit Values with No 8-bit Mapping Sorted by 10-Bit Value

10B Dec	10 B	COMMENT
0	00 0000 0000	ILLEGAL
1	00 0000 0001	ILLEGAL
2	00 0000 0010	ILLEGAL
3	00 0000 0011	ILLEGAL
4	00 0000 0100	ILLEGAL
5	00 0000 0101	ILLEGAL
6	00 0000 0110	ILLEGAL
7	00 0000 0111	ILLEGAL
8	00 0000 1000	ILLEGAL
9	00 0000 1001	ILLEGAL
10	00 0000 1010	ILLEGAL
11	00 0000 1011	ILLEGAL
12	00 0000 1100	ILLEGAL
13	00 0000 1101	ILLEGAL
14	00 0000 1110	ILLEGAL
15	00 0000 1111	ILLEGAL
16	00 0001 0000	ILLEGAL
17	00 0001 0001	ILLEGAL
18	00 0001 0010	ILLEGAL
19	00 0001 0011	ILLEGAL
20	00 0001 0100	ILLEGAL
21	00 0001 0101	ILLEGAL
22	00 0001 0110	ILLEGAL
23	00 0001 0111	ILLEGAL
24	00 0001 1000	ILLEGAL
25	00 0001 1001	ILLEGAL
26	00 0001 1010	ILLEGAL
27	00 0001 1011	ILLEGAL
28	00 0001 1100	ILLEGAL
29	00 0001 1101	ILLEGAL
30	00 0001 1110	ILLEGAL
31	00 0001 1111	ILLEGAL
32	00 0010 0000	ILLEGAL
33	00 0010 0001	ILLEGAL
34	00 0010 0010	ILLEGAL
35	00 0010 0011	ILLEGAL
36	00 0010 0100	ILLEGAL
37	00 0010 0101	ILLEGAL
38	00 0010 0110	ILLEGAL
39	00 0010 0111	ILLEGAL
40	00 0010 1000	ILLEGAL
41	00 0010 1001	ILLEGAL
42	00 0010 1010	ILLEGAL
43	00 0010 1011	ILLEGAL
44	00 0010 1100	ILLEGAL
45	00 0010 1101	ILLEGAL
46	00 0010 1110	ILLEGAL
47	00 0010 1111	ILLEGAL
48	00 0011 0000	ILLEGAL
49	00 0011 0001	ILLEGAL
50	00 0011 0010	ILLEGAL
51	00 0011 0011	ILLEGAL
52	00 0011 0100	ILLEGAL
53	00 0011 0101	ILLEGAL
54	00 0011 0110	ILLEGAL
55	00 0011 0111	ILLEGAL
56	00 0011 1000	ILLEGAL
57	00 0011 1001	ILLEGAL
58	00 0011 1010	ILLEGAL
59	00 0011 1011	ILLEGAL
60	00 0011 1100	ILLEGAL
61	00 0011 1101	ILLEGAL
62	00 0011 1110	ILLEGAL
63	00 0011 1111	ILLEGAL
64	00 0100 0000	ILLEGAL
65	00 0100 0001	ILLEGAL
66	00 0100 0010	ILLEGAL
67	00 0100 0011	ILLEGAL
68	00 0100 0100	ILLEGAL
69	00 0100 0101	ILLEGAL
70	00 0100 0110	ILLEGAL
71	00 0100 0111	ILLEGAL
72	00 0100 1000	ILLEGAL
73	00 0100 1001	ILLEGAL
74	00 0100 1010	ILLEGAL
75	00 0100 1011	ILLEGAL
76	00 0100 1100	ILLEGAL
77	00 0100 1101	ILLEGAL
78	00 0100 1110	ILLEGAL
79	00 0100 1111	ILLEGAL
80	00 0101 0000	ILLEGAL
81	00 0101 0001	ILLEGAL
82	00 0101 0010	ILLEGAL
83	00 0101 0011	ILLEGAL
84	00 0101 0100	ILLEGAL
88	00 0101 1000	ILLEGAL
95	00 0101 1111	ILLEGAL
96	00 0110 0000	ILLEGAL
97	00 0110 0001	ILLEGAL
98	00 0110 0010	ILLEGAL
99	00 0110 0011	ILLEGAL
100	00 0110 0100	ILLEGAL
103	00 0110 0111	ILLEGAL
104	00 0110 1000	ILLEGAL
111	00 0110 1111	ILLEGAL
112	00 0111 0000	ILLEGAL
119	00 0111 0111	ILLEGAL
120	00 0111 1000	ILLEGAL
123	00 0111 1011	ILLEGAL
124	00 0111 1100	ILLEGAL
125	00 0111 1101	ILLEGAL
126	00 0111 1110	ILLEGAL
127	00 0111 1111	ILLEGAL
128	00 1000 0000	ILLEGAL
129	00 1000 0001	ILLEGAL
130	00 1000 0010	ILLEGAL
131	00 1000 0011	ILLEGAL
132	00 1000 0100	ILLEGAL
133	00 1000 0101	ILLEGAL
134	00 1000 0110	ILLEGAL
135	00 1000 0111	ILLEGAL
136	00 1000 1000	ILLEGAL
137	00 1000 1001	ILLEGAL
138	00 1000 1010	ILLEGAL
139	00 1000 1011	ILLEGAL
140	00 1000 1100	ILLEGAL
141	00 1000 1101	ILLEGAL

142 00 1000 1110 ILLEGAL
143 00 1000 1111 ILLEGAL
144 00 1001 0000 ILLEGAL
145 00 1001 0001 ILLEGAL
146 00 1001 0010 ILLEGAL
147 00 1001 0011 ILLEGAL
148 00 1001 0100 ILLEGAL
152 00 1001 1000 ILLEGAL
159 00 1001 1111 ILLEGAL
160 00 1010 0000 ILLEGAL
161 00 1010 0001 ILLEGAL
162 00 1010 0010 ILLEGAL
163 00 1010 0011 ILLEGAL
164 00 1010 0100 ILLEGAL
167 00 1010 0111 ILLEGAL
168 00 1010 1000 ILLEGAL
175 00 1010 1111 ILLEGAL
176 00 1011 0000 ILLEGAL
184 00 1011 1000 ILLEGAL
190 00 1011 1110 ILLEGAL
191 00 1011 1111 ILLEGAL
192 00 1100 0000 ILLEGAL
193 00 1100 0001 ILLEGAL
194 00 1100 0010 ILLEGAL
195 00 1100 0011 ILLEGAL
196 00 1100 0100 ILLEGAL
199 00 1100 0111 ILLEGAL
200 00 1100 1000 ILLEGAL
207 00 1100 1111 ILLEGAL
208 00 1101 0000 ILLEGAL
215 00 1101 0111 ILLEGAL
216 00 1101 1000 ILLEGAL
223 00 1101 1111 ILLEGAL
224 00 1110 0000 ILLEGAL
231 00 1110 0111 ILLEGAL
232 00 1110 1000 ILLEGAL
239 00 1110 1111 ILLEGAL
240 00 1111 0000 ILLEGAL
241 00 1111 0001 ILLEGAL
247 00 1111 0111 ILLEGAL
251 00 1111 1011 ILLEGAL
252 00 1111 1100 ILLEGAL
253 00 1111 1101 ILLEGAL
254 00 1111 1110 ILLEGAL
255 00 1111 1111 ILLEGAL
256 01 0000 0000 ILLEGAL
257 01 0000 0001 ILLEGAL
258 01 0000 0010 ILLEGAL
259 01 0000 0011 ILLEGAL
260 01 0000 0100 ILLEGAL
261 01 0000 0101 ILLEGAL
262 01 0000 0110 ILLEGAL
263 01 0000 0111 ILLEGAL
264 01 0000 1000 ILLEGAL
265 01 0000 1001 ILLEGAL
266 01 0000 1010 ILLEGAL
267 01 0000 1011 ILLEGAL
268 01 0000 1100 ILLEGAL
269 01 0000 1101 ILLEGAL
270 01 0000 1110 ILLEGAL
271 01 0000 1111 ILLEGAL
272 01 0001 0000 ILLEGAL
273 01 0001 0001 ILLEGAL
274 01 0001 0010 ILLEGAL
275 01 0001 0011 ILLEGAL
276 01 0001 0100 ILLEGAL
280 01 0001 1000 ILLEGAL
287 01 0001 1111 ILLEGAL
288 01 0010 0000 ILLEGAL
289 01 0010 0001 ILLEGAL
290 01 0010 0010 ILLEGAL
291 01 0010 0011 ILLEGAL
292 01 0010 0100 ILLEGAL
295 01 0010 0111 ILLEGAL
296 01 0010 1000 ILLEGAL
303 01 0010 1111 ILLEGAL
304 01 0011 0000 ILLEGAL
312 01 0011 1000 ILLEGAL
318 01 0011 1110 ILLEGAL
319 01 0011 1111 ILLEGAL
320 01 0100 0000 ILLEGAL
321 01 0100 0001 ILLEGAL
322 01 0100 0010 ILLEGAL
323 01 0100 0011 ILLEGAL
324 01 0100 0100 ILLEGAL
327 01 0100 0111 ILLEGAL
328 01 0100 1000 ILLEGAL
335 01 0100 1111 ILLEGAL
336 01 0101 0000 ILLEGAL
343 01 0101 0111 ILLEGAL
344 01 0101 1000 ILLEGAL
351 01 0101 1111 ILLEGAL
352 01 0110 0000 ILLEGAL
359 01 0110 0111 ILLEGAL
360 01 0110 1000 ILLEGAL
367 01 0110 1111 ILLEGAL
368 01 0111 0000 ILLEGAL
375 01 0111 0111 ILLEGAL
376 01 0111 1000 ILLEGAL
379 01 0111 1011 ILLEGAL
380 01 0111 1100 ILLEGAL
381 01 0111 1101 ILLEGAL
382 01 0111 1110 ILLEGAL
383 01 0111 1111 ILLEGAL
384 01 1000 0000 ILLEGAL
385 01 1000 0001 ILLEGAL
386 01 1000 0010 ILLEGAL
387 01 1000 0011 ILLEGAL
388 01 1000 0100 ILLEGAL
391 01 1000 0111 ILLEGAL
392 01 1000 1000 ILLEGAL
399 01 1000 1111 ILLEGAL
400 01 1001 0000 ILLEGAL
407 01 1001 0111 ILLEGAL
408 01 1001 1000 ILLEGAL
415 01 1001 1111 ILLEGAL
416 01 1010 0000 ILLEGAL
423 01 1010 0111 ILLEGAL
424 01 1010 1000 ILLEGAL
431 01 1010 1111 ILLEGAL
432 01 1011 0000 ILLEGAL
439 01 1011 0111 ILLEGAL
440 01 1011 1000 ILLEGAL
443 01 1011 1011 ILLEGAL
444 01 1011 1100 ILLEGAL
445 01 1011 1101 ILLEGAL
446 01 1011 1110 ILLEGAL
447 01 1011 1111 ILLEGAL
448 01 1100 0000 ILLEGAL
449 01 1100 0001 ILLEGAL

455	01 1100 0111	ILLEGAL
463	01 1100 1111	ILLEGAL
464	01 1101 0000	ILLEGAL
471	01 1101 0111	ILLEGAL
472	01 1101 1000	ILLEGAL
475	01 1101 1011	ILLEGAL
476	01 1101 1100	ILLEGAL
477	01 1101 1101	ILLEGAL
478	01 1101 1110	ILLEGAL
479	01 1101 1111	ILLEGAL
480	01 1110 0000	ILLEGAL
487	01 1110 0111	ILLEGAL
491	01 1110 1011	ILLEGAL
492	01 1110 1100	ILLEGAL
493	01 1110 1101	ILLEGAL
494	01 1110 1110	ILLEGAL
495	01 1110 1111	ILLEGAL
496	01 1111 0000	ILLEGAL
497	01 1111 0001	ILLEGAL
498	01 1111 0010	ILLEGAL
499	01 1111 0011	ILLEGAL
500	01 1111 0100	ILLEGAL
501	01 1111 0101	ILLEGAL
502	01 1111 0110	ILLEGAL
503	01 1111 0111	ILLEGAL
504	01 1111 1000	ILLEGAL
505	01 1111 1001	ILLEGAL
506	01 1111 1010	ILLEGAL
507	01 1111 1011	ILLEGAL
508	01 1111 1100	ILLEGAL
509	01 1111 1101	ILLEGAL
510	01 1111 1110	ILLEGAL
511	01 1111 1111	ILLEGAL
512	10 0000 0000	ILLEGAL
513	10 0000 0001	ILLEGAL
514	10 0000 0010	ILLEGAL
515	10 0000 0011	ILLEGAL
516	10 0000 0100	ILLEGAL
517	10 0000 0101	ILLEGAL
518	10 0000 0110	ILLEGAL
519	10 0000 0111	ILLEGAL
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525	10 0000 1101	ILLEGAL
526	10 0000 1110	ILLEGAL
527	10 0000 1111	ILLEGAL
528	10 0001 0000	ILLEGAL
529	10 0001 0001	ILLEGAL
530	10 0001 0010	ILLEGAL
531	10 0001 0011	ILLEGAL
532	10 0001 0100	ILLEGAL
536	10 0001 1000	ILLEGAL
543	10 0001 1111	ILLEGAL
544	10 0010 0000	ILLEGAL
545	10 0010 0001	ILLEGAL
546	10 0010 0010	ILLEGAL
547	10 0010 0011	ILLEGAL
548	10 0010 0100	ILLEGAL
551	10 0010 0111	ILLEGAL
552	10 0010 1000	ILLEGAL
559	10 0010 1111	ILLEGAL
560	10 0011 0000	ILLEGAL
568	10 0011 1000	ILLEGAL
574	10 0011 1110	ILLEGAL
575	10 0011 1111	ILLEGAL
576	10 0100 0000	ILLEGAL
577	10 0100 0001	ILLEGAL
578	10 0100 0010	ILLEGAL
579	10 0100 0011	ILLEGAL
580	10 0100 0100	ILLEGAL
583	10 0100 0111	ILLEGAL
584	10 0100 1000	ILLEGAL
591	10 0100 1111	ILLEGAL
592	10 0101 0000	ILLEGAL
599	10 0101 0111	ILLEGAL
600	10 0101 1000	ILLEGAL
607	10 0101 1111	ILLEGAL
608	10 0110 0000	ILLEGAL
615	10 0110 0111	ILLEGAL
616	10 0110 1000	ILLEGAL
623	10 0110 1111	ILLEGAL
624	10 0111 0000	ILLEGAL
631	10 0111 0111	ILLEGAL
632	10 0111 1000	ILLEGAL
635	10 0111 1011	ILLEGAL
636	10 0111 1100	ILLEGAL
637	10 0111 1101	ILLEGAL
638	10 0111 1110	ILLEGAL
639	10 0111 1111	ILLEGAL
640	10 1000 0000	ILLEGAL
641	10 1000 0001	ILLEGAL
642	10 1000 0010	ILLEGAL
643	10 1000 0011	ILLEGAL
644	10 1000 0100	ILLEGAL
647	10 1000 0111	ILLEGAL
648	10 1000 1000	ILLEGAL
655	10 1000 1111	ILLEGAL
656	10 1001 0000	ILLEGAL
663	10 1001 0111	ILLEGAL
664	10 1001 1000	ILLEGAL
671	10 1001 1111	ILLEGAL
672	10 1010 0000	ILLEGAL
679	10 1010 0111	ILLEGAL
680	10 1010 1000	ILLEGAL
687	10 1010 1111	ILLEGAL
688	10 1011 0000	ILLEGAL
695	10 1011 0111	ILLEGAL
696	10 1011 1000	ILLEGAL
699	10 1011 1011	ILLEGAL
700	10 1011 1100	ILLEGAL
701	10 1011 1101	ILLEGAL
702	10 1011 1110	ILLEGAL
703	10 1011 1111	ILLEGAL
704	10 1100 0000	ILLEGAL
705	10 1100 0001	ILLEGAL
711	10 1100 0111	ILLEGAL
719	10 1100 1111	ILLEGAL
720	10 1101 0000	ILLEGAL
727	10 1101 0111	ILLEGAL
728	10 1101 1000	ILLEGAL
731	10 1101 1011	ILLEGAL
732	10 1101 1100	ILLEGAL
733	10 1101 1101	ILLEGAL
734	10 1101 1110	ILLEGAL
735	10 1101 1111	ILLEGAL
736	10 1110 0000	ILLEGAL
743	10 1110 0111	ILLEGAL

747	10 1110 1011	ILLEGAL
748	10 1110 1100	ILLEGAL
749	10 1110 1101	ILLEGAL
750	10 1110 1110	ILLEGAL
751	10 1110 1111	ILLEGAL
752	10 1111 0000	ILLEGAL
753	10 1111 0001	ILLEGAL
754	10 1111 0010	ILLEGAL
755	10 1111 0011	ILLEGAL
756	10 1111 0100	ILLEGAL
757	10 1111 0101	ILLEGAL
758	10 1111 0110	ILLEGAL
759	10 1111 0111	ILLEGAL
760	10 1111 1000	ILLEGAL
761	10 1111 1001	ILLEGAL
762	10 1111 1010	ILLEGAL
763	10 1111 1011	ILLEGAL
764	10 1111 1100	ILLEGAL
765	10 1111 1101	ILLEGAL
766	10 1111 1110	ILLEGAL
767	10 1111 1111	ILLEGAL
768	11 0000 0000	ILLEGAL
769	11 0000 0001	ILLEGAL
770	11 0000 0010	ILLEGAL
771	11 0000 0011	ILLEGAL
772	11 0000 0100	ILLEGAL
776	11 0000 1000	ILLEGAL
782	11 0000 1110	ILLEGAL
783	11 0000 1111	ILLEGAL
784	11 0001 0000	ILLEGAL
791	11 0001 0111	ILLEGAL
792	11 0001 1000	ILLEGAL
799	11 0001 1111	ILLEGAL
800	11 0010 0000	ILLEGAL
807	11 0010 0111	ILLEGAL
808	11 0010 1000	ILLEGAL
815	11 0010 1111	ILLEGAL
816	11 0011 0000	ILLEGAL
823	11 0011 0111	ILLEGAL
824	11 0011 1000	ILLEGAL
827	11 0011 1011	ILLEGAL
828	11 0011 1100	ILLEGAL
829	11 0011 1101	ILLEGAL
830	11 0011 1110	ILLEGAL
831	11 0011 1111	ILLEGAL
832	11 0100 0000	ILLEGAL
833	11 0100 0001	ILLEGAL
839	11 0100 0111	ILLEGAL
847	11 0100 1111	ILLEGAL
848	11 0101 0000	ILLEGAL
855	11 0101 0111	ILLEGAL
856	11 0101 1000	ILLEGAL
859	11 0101 1011	ILLEGAL
860	11 0101 1100	ILLEGAL
861	11 0101 1101	ILLEGAL
862	11 0101 1110	ILLEGAL
863	11 0101 1111	ILLEGAL
864	11 0110 0000	ILLEGAL
871	11 0110 0111	ILLEGAL
875	11 0110 1011	ILLEGAL
876	11 0110 1100	ILLEGAL
877	11 0110 1101	ILLEGAL
878	11 0110 1110	ILLEGAL
879	11 0110 1111	ILLEGAL
880	11 0111 0000	ILLEGAL
881	11 0111 0001	ILLEGAL
882	11 0111 0010	ILLEGAL
883	11 0111 0011	ILLEGAL
884	11 0111 0100	ILLEGAL
885	11 0111 0101	ILLEGAL
886	11 0111 0110	ILLEGAL
887	11 0111 0111	ILLEGAL
888	11 0111 1000	ILLEGAL
889	11 0111 1001	ILLEGAL
890	11 0111 1010	ILLEGAL
891	11 0111 1011	ILLEGAL
892	11 0111 1100	ILLEGAL
893	11 0111 1101	ILLEGAL
894	11 0111 1110	ILLEGAL
895	11 0111 1111	ILLEGAL
896	11 1000 0000	ILLEGAL
897	11 1000 0001	ILLEGAL
898	11 1000 0010	ILLEGAL
899	11 1000 0011	ILLEGAL
900	11 1000 0100	ILLEGAL
903	11 1000 0111	ILLEGAL
904	11 1000 1000	ILLEGAL
911	11 1000 1111	ILLEGAL
912	11 1001 0000	ILLEGAL
919	11 1001 0111	ILLEGAL
920	11 1001 1000	ILLEGAL
923	11 1001 1011	ILLEGAL
924	11 1001 1100	ILLEGAL
925	11 1001 1101	ILLEGAL
926	11 1001 1110	ILLEGAL
927	11 1001 1111	ILLEGAL
928	11 1010 0000	ILLEGAL
935	11 1010 0111	ILLEGAL
939	11 1010 1011	ILLEGAL
940	11 1010 1100	ILLEGAL
941	11 1010 1101	ILLEGAL
942	11 1010 1110	ILLEGAL
943	11 1010 1111	ILLEGAL
944	11 1011 0000	ILLEGAL
945	11 1011 0001	ILLEGAL
946	11 1011 0010	ILLEGAL
947	11 1011 0011	ILLEGAL
948	11 1011 0100	ILLEGAL
949	11 1011 0101	ILLEGAL
950	11 1011 0110	ILLEGAL
951	11 1011 0111	ILLEGAL
952	11 1011 1000	ILLEGAL
953	11 1011 1001	ILLEGAL
954	11 1011 1010	ILLEGAL
955	11 1011 1011	ILLEGAL
956	11 1011 1100	ILLEGAL
957	11 1011 1101	ILLEGAL
958	11 1011 1110	ILLEGAL
959	11 1011 1111	ILLEGAL
960	11 1100 0000	ILLEGAL
961	11 1100 0001	ILLEGAL
962	11 1100 0010	ILLEGAL
963	11 1100 0011	ILLEGAL
964	11 1100 0100	ILLEGAL
965	11 1100 0101	ILLEGAL
966	11 1100 0110	ILLEGAL
967	11 1100 0111	ILLEGAL
968	11 1100 1000	ILLEGAL
969	11 1100 1001	ILLEGAL
970	11 1100 1010	ILLEGAL

971	11 1100 1011	ILLEGAL
972	11 1100 1100	ILLEGAL
973	11 1100 1101	ILLEGAL
974	11 1100 1110	ILLEGAL
975	11 1100 1111	ILLEGAL
976	11 1101 0000	ILLEGAL
977	11 1101 0001	ILLEGAL
978	11 1101 0010	ILLEGAL
979	11 1101 0011	ILLEGAL
980	11 1101 0100	ILLEGAL
981	11 1101 0101	ILLEGAL
982	11 1101 0110	ILLEGAL
983	11 1101 0111	ILLEGAL
984	11 1101 1000	ILLEGAL
985	11 1101 1001	ILLEGAL
986	11 1101 1010	ILLEGAL
987	11 1101 1011	ILLEGAL
988	11 1101 1100	ILLEGAL
989	11 1101 1101	ILLEGAL
990	11 1101 1110	ILLEGAL
991	11 1101 1111	ILLEGAL
992	11 1110 0000	ILLEGAL
993	11 1110 0001	ILLEGAL
994	11 1110 0010	ILLEGAL
995	11 1110 0011	ILLEGAL
996	11 1110 0100	ILLEGAL
997	11 1110 0101	ILLEGAL
998	11 1110 0110	ILLEGAL
999	11 1110 0111	ILLEGAL
1000	11 1110 1000	ILLEGAL
1001	11 1110 1001	ILLEGAL
1002	11 1110 1010	ILLEGAL
1003	11 1110 1011	ILLEGAL
1004	11 1110 1100	ILLEGAL
1005	11 1110 1101	ILLEGAL
1006	11 1110 1110	ILLEGAL
1007	11 1110 1111	ILLEGAL
1008	11 1111 0000	ILLEGAL
1009	11 1111 0001	ILLEGAL
1010	11 1111 0010	ILLEGAL
1011	11 1111 0011	ILLEGAL
1012	11 1111 0100	ILLEGAL
1013	11 1111 0101	ILLEGAL
1014	11 1111 0110	ILLEGAL
1015	11 1111 0111	ILLEGAL
1016	11 1111 1000	ILLEGAL
1017	11 1111 1001	ILLEGAL
1018	11 1111 1010	ILLEGAL
1019	11 1111 1011	ILLEGAL
1020	11 1111 1100	ILLEGAL
1021	11 1111 1101	ILLEGAL
1022	11 1111 1110	ILLEGAL
1023	11 1111 1111	ILLEGAL

The following table lists:

Legal 10-Bit Values Sorted by 8-Bit Hex Code

10B Dec	8B Dec	ASCII+	HEX	Previous Disparity	Data Byte FC Name	10 B	COMMENT
1013	50	NUL	00	RD +	D0.0	01 1000 1011	
628	0	NUL	00	RD--	D0.0	10 0111 0100	
468	1	SOH	01	RD--	D1.0	01 1101 0100	
555	1	SOH	01	RD +	D1.0	10 0010 1011	
299	2	STX	02	RD +	D2.0	01 0010 1011	
724	2	STX	02	RD--	D2.0	10 1101 0100	
788	3	ETX	03	RD +	D3.0	11 0001 0100	
795	3	ETX	03	RD--	D3.0	11 0001 1011	
171	4	EOT	04	RD +	D4.0	00 1010 1011	
852	4	EOT	04	RD--	D4.0	11 0101 0100	
660	5	ENQ	05	RD +	D5.0	10 1001 0100	
667	5	ENQ	05	RD--	D5.0	10 1001 1011	
404	6	ACK	06	RD +	D6.0	01 1001 0100	
411	6	ACK	06	RD--	D6.0	01 1001 1011	
116	7	BEL	07	RD +	D7.0	00 0111 0100	
907	7	BEL	07	RD--	D7.0	11 1000 1011	
107	8	BS	08	RD +	D8.0	00 0110 1011	
916	8	BS	08	RD--	D8.0	11 1001 0100	
596	9	HT	09	RD +	D9.0	10 0101 0100	
603	9	HT	09	RD--	D9.0	10 0101 1011	
436	16	DLE	10	RD--	D16.0	01 1011 0100	
587	16	DLE	10	RD +	D16.0	10 0100 1011	
564	17	DC1	11	RD +	D17.0	10 0011 0100	
571	17	DC1	11	RD--	D17.0	10 0011 1011	
308	18	DC2	12	RD +	D18.0	01 0011 0100	
315	18	DC2	12	RD--	D18.0	01 0011 1011	
804	19	DC3	13	RD +	D19.0	11 0010 0100	
811	19	DC3	13	RD--	D19.0	11 0010 1011	
180	20	DC4	14	RD +	D20.0	00 1011 0100	
187	20	DC4	14	RD--	D20.0	00 1011 1011	
676	21	NAK	15	RD +	D21.0	10 1010 0100	
683	21	NAK	15	RD--	D21.0	10 1010 1011	
420	22	SYN	16	RD +	D22.0	01 1010 0100	
427	22	SYN	16	RD--	D22.0	01 1010 1011	
91	23	ETB	17	RD +	D23.0	00 0101 1011	
932	23	ETB	17	RD--	D23.0	11 1010 0100	
203	24	CAN	18	RD +	D24.0	00 1100 1011	
820	24	CAN	18	RD--	D24.0	11 0011 0100	
612	25	EM	19	RD +	D25.0	10 0110 0100	
619	25	EM	19	RD--	D25.0	10 0110 1011	
393	32	SPACE	20	RD +	D0.1	01 1000 1001	
633	32	SPACE	20	RD--	D0.1	10 0111 1001	
473	33	!	21	RD--	D1.1	01 1101 1001	
553	33	!	21	RD +	D1.1	10 0010 1001	
297	34	"	22	RD +	D2.1	01 0010 1001	
729	34	"	22	RD--	D2.1	10 1101 1001	
793	35	#	23	RD+/-	D3.1	11 0001 1001	
169	36	$	24	RD +	D4.1	00 1010 1001	
857	36	$	24	RD--	D4.1	11 0101 1001	
665	37	%	25	RD+/-	D5.1	10 1001 1001	
409	38	&	26	RD+/-	D6.1	01 1001 1001	
121	39	'	27	RD +	D7.1	00 0111 1001	
905	39	'	27	RD--	D7.1	11 1000 1001	
105	40	(	28	RD +	D8.1	00 0110 1001	
921	40	(	28	RD--	D8.1	11 1001 1001	
601	41	)	29	RD+/-	D9.1	10 0101 1001	
441	48	0	30	RD--	D16.1	01 1011 1001	
585	48	0	30	RD +	D16.1	10 0100 1001	
569	49	1	31	RD+/-	D17.1	10 0011 1001	
313	50	2	32	RD+/-	D18.1	01 0011 1001	
809	51	3	33	RD+/-	D19.1	11 0010 1001	
185	52	4	34	RD+/-	D20.1	00 1011 1001	
681	53	5	35	RD+/-	D21.1	10 1010 1001	
425	54	6	36	RD+/-	D22.1	01 1010 1001	
89	55	7	37	RD +	D23.1	00 0101 1001	
937	55	7	37	RD--	D23.1	11 1010 1001	
201	56	8	38	RD +	D24.1	00 1100 1001	
825	56	8	38	RD--	D24.1	11 0011 1001	
617	57	9	39	RD+/-	D25.1	10 0110 1001	
389	64	@	40	RD +	D0.2	01 1000 0101	
629	64	@	40	RD--	D0.2	10 0111 0101	
469	65	A	41	RD--	D1.2	01 1101 0101	
549	65	A	41	RD +	D1.2	10 0010 0101	
293	66	B	42	RD +	D2.2	01 0010 0101	
725	66	B	42	RD--	D2.2	10 1101 0101	
789	67	C	43	RD+/-	D3.2	11 0001 0101	
165	68	D	44	RD +	D4.2	00 1010 0101	
853	68	D	44	RD--	D4.2	11 0101 0101	
661	69	E	45	RD+/-	D5.2	10 1001 0101	
405	70	F	46	RD+/-	D6.2	01 1001 0101	
117	71	G	47	RD +	D7.2	00 0111 0101	
901	71	G	47	RD--	D7.2	11 1000 0101	
101	72	H	48	RD +	D8.2	00 0110 0101	
917	72	H	48	RD--	D8.2	11 1001 0101	
597	73	I	49	RD+/-	D9.2	10 0101 0101	
437	80	P	50	RD--	D16.2	01 1011 0101	
581	80	P	50	RD +	D16.2	10 0100 0101	
565	81	Q	51	RD+/-	D17.2	10 0011 0101	
309	82	R	52	RD+/-	D18.2	01 0011 0101	
805	83	S	53	RD+/-	D19.2	11 0010 0101	
181	84	T	54	RD+/-	D20.2	00 1011 0101	
677	85	U	55	RD+/-	D21.2	10 1010 0101	
421	86	V	56	RD+/-	D22.2	01 1010 0101	
85	87	W	57	RD +	D23.2	00 0101 0101	
933	87	W	57	RD--	D23.2	11 1010 0101	
197	88	X	58	RD +	D24.2	00 1100 0101	
821	88	X	58	RD--	D24.2	11 0011 0101	
613	89	Y	59	RD+/-	D25.2	10 0110 0101	
396	96	`	60	RD +	D0.3	01 1000 1100	
627	96	`	60	RD--	D0.3	10 0111 0011	
467	97	a	61	RD--	D1.3	01 1101 0011	
556	97	a	61	RD +	D1.3	10 0010 1100	
300	98	b	62	RD +	D2.3	01 0010 1100	
723	98	b	62	RD--	D2.3	10 1101 0011	
787	99	c	63	RD +	D3.3	11 0001 0011	
796	99	c	63	RD--	D3.3	11 0001 1100	
172	100	d	64	RD +	D4.3	00 1010 1100	
851	100	d	64	RD--	D4.3	11 0101 0011	

659	101	e	65	RD +	D5.3	10 1001 0011
668	101	e	65	RD--	D5.3	10 1001 1100
403	102	f	66	RD +	D6.3	01 1001 0011
412	102	f	66	RD--	D6.3	01 1001 1100
115	103	g	67	RD +	D7.3	00 0111 0011
908	103	g	67	RD--	D7.3	11 1000 1100
108	104	h	68	RD +	D8.3	00 0110 1100
915	104	h	68	RD--	D8.3	11 1001 0011
595	105	i	69	RD +	D9.3	10 0101 0011
604	105	i	69	RD--	D9.3	10 0101 1100
435	112	p	70	RD--	D16.3	01 1011 0011
588	112	p	70	RD +	D16.3	10 0100 1100
563	113	q	71	RD +	D17.3	10 0011 0011
572	113	q	71	RD--	D17.3	10 0011 1100
307	114	r	72	RD +	D18.3	01 0011 0011
316	114	r	72	RD--	D18.3	01 0011 1100
803	115	s	73	RD +	D19.3	11 0010 0011
812	115	s	73	RD--	D19.3	11 0010 1100
179	116	t	74	RD +	D20.3	00 1011 0011
188	116	t	74	RD--	D20.3	00 1011 1100
675	117	u	75	RD +	D21.3	10 1010 0011
684	117	u	75	RD--	D21.3	10 1010 1100
419	118	v	76	RD +	D22.3	01 1010 0011
428	118	v	76	RD--	D22.3	01 1010 1100
92	119	w	77	RD +	D23.3	00 0101 1100
931	119	w	77	RD--	D23.3	11 1010 0011
204	120	x	78	RD +	D24.3	00 1100 1100
819	120	x	78	RD--	D24.3	11 0011 0011
611	121	y	79	RD +	D25.3	10 0110 0011
620	121	y	79	RD--	D25.3	10 0110 1100
397	128	_	80	RD +	D0.4	01 1000 1101
626	128	_	80	RD--	D0.4	10 0111 0010
466	129	_	81	RD--	D1.4	01 1101 0010
557	129	_	81	RD +	D1.4	10 0010 1101
301	130	‚	82	RD +	D2.4	01 0010 1101
722	130	‚	82	RD--	D2.4	10 1101 0010
786	131	*f*	83	RD +	D3.4	11 0001 0010
797	131	*f*	83	RD--	D3.4	11 0001 1101
173	132	„	84	RD +	D4.4	00 1010 1101
850	132	„	84	RD--	D4.4	11 0101 0010
658	133	…	85	RD +	D5.4	10 1001 0010
669	133	…	85	RD--	D5.4	10 1001 1101
402	134	†	86	RD +	D6.4	01 1001 0010
413	134	†	86	RD--	D6.4	01 1001 1101
114	135	‡	87	RD +	D7.4	00 0111 0010
909	135	‡	87	RD--	D7.4	11 1000 1101
109	136	ˆ	88	RD +	D8.4	00 0110 1101
914	136	ˆ	88	RD--	D8.4	11 1001 0010
594	137	‰	89	RD +	D9.4	10 0101 0010
605	137	‰	89	RD--	D9.4	10 0101 1101
434	144	_	90	RD--	D16.4	01 1011 0010
589	144	_	90	RD +	D16.4	10 0100 1101
562	145	‘	91	RD +	D17.4	10 0011 0010
573	145	‘	91	RD--	D17.4	10 0011 1101
306	146	’	92	RD +	D18.4	01 0011 0010
317	146	’	92	RD--	D18.4	01 0011 1101
802	147	“	93	RD +	D19.4	11 0010 0010
813	147	“	93	RD--	D19.4	11 0010 1101
178	148	”	94	RD +	D20.4	00 1011 0010
189	148	”	94	RD--	D20.4	00 1011 1101
674	149	•	95	RD +	D21.4	10 1010 0010
685	149	•	95	RD--	D21.4	10 1010 1101
418	150	–	96	RD +	D22.4	01 1010 0010
429	150	–	96	RD--	D22.4	01 1010 1101
93	151	—	97	RD +	D23.4	00 0101 1101
930	151	—	97	RD--	D23.4	11 1010 0010
205	152	˜	98	RD +	D24.4	00 1100 1101
818	152	˜	98	RD--	D24.4	11 0011 0010
610	153	™	99	RD +	D25.4	10 0110 0010
621	153	™	99	RD--	D25.4	10 0110 1101
340	10	LF	0A	RD +	D10.0	01 0101 0100
347	10	LF	0A	RD--	D10.0	01 0101 1011
836	11	VT	0B	RD +	D11.0	11 0100 0100
843	11	VT	0B	RD--	D11.0	11 0100 1011
212	12	FF	0C	RD +	D12.0	00 1101 0100
219	12	FF	0C	RD--	D12.0	00 1101 1011
708	13	CR	0D	RD +	D13.0	10 1100 0100
715	13	CR	0D	RD--	D13.0	10 1100 1011
452	14	SO	0E	RD +	D14.0	01 1100 0100
459	14	SO	0E	RD--	D14.0	01 1100 1011
372	15	SI	0F	RD--	D15.0	01 0111 0100
651	15	SI	0F	RD +	D15.0	10 1000 1011
356	26	SUB	1A	RD +	D26.0	01 0110 0100
363	26	SUB	1A	RD--	D26.0	01 0110 1011
155	27	ESC	1B	RD +	D27.0	00 1001 1011
868	27	ESC	1B	RD--	D27.0	11 0110 0100
228	28	FS	1C	RD +	D28.0	00 1110 0100
235	28	FS	1C	RD--	D28.0	00 1110 1011
244	28	FS	1C	RD --	K28.0	00 1111 0100 Reserved*
779	28	FS	1C	RD +	K28.0	11 0000 1011
283	29	GS	1D	RD +	D29.0	01 0001 1011
740	29	GS	1D	RD--	D29.0	10 1110 0100
484	30	RS	1E	RD--	D30.0	01 1110 0100
539	30	RS	1E	RD +	D30.0	10 0001 1011
331	31	US	1F	RD +	D31.0	01 0100 1011
692	31	US	1F	RD--	D31.0	10 1011 0100
345	42	*	2A	RD+/--	D10.1	01 0101 1001
841	43	+	2B	RD+/--	D11.1	11 0100 1001
217	44	,	2C	RD+/--	D12.1	00 1101 1001
713	45	-	2D	RD+/--	D13.1	10 1100 1001
457	46	.	2E	RD+/--	D14.1	01 1100 1001
377	47	/	2F	RD--	D15.1	01 0111 1001
649	47	/	2F	RD +	D15.1	10 1000 1001
361	58	:	3A	RD+/--	D26.1	01 0110 1001
153	59	;	3B	RD +	D27.1	00 1001 1001
873	59	;	3B	RD--	D27.1	11 0110 1001
233	60	<	3C	RD+/--	D28.1	00 1110 1001
249	60	<	3C	RD --	K28.1	00 1111 1001 Reserved*
774	60	<	3C	RD +	K28.1	11 0000 0110
281	61	=	3D	RD +	D29.1	01 0001 1001
745	61	=	3D	RD--	D29.1	10 1110 1001
489	62	>	3E	RD--	D30.1	01 1110 1001
537	62	>	3E	RD +	D30.1	10 0001 1001
329	63	?	3F	RD +	D31.1	01 0100 1001
697	63	?	3F	RD--	D31.1	10 1011 1001
341	74	J	4A	RD+/--	D10.2	01 0101 0101
837	75	K	4B	RD+/--	D11.2	11 0100 0101
213	76	L	4C	RD+/--	D12.2	00 1101 0101
709	77	M	4D	RD+/--	D13.2	10 1100 0101
453	78	N	4E	RD+/--	D14.2	01 1100 0101
373	79	O	4F	RD--	D15.2	01 0111 0101
645	79	O	4F	RD +	D15.2	10 1000 0101
357	90	Z	5A	RD+/--	D26.2	01 0110 0101
149	91	[	5B	RD +	D27.2	00 1001 0101
869	91	[	5B	RD--	D27.2	11 0110 0101
229	92	\	5C	RD+/--	D28.2	00 1110 0101
245	92	\	5C	RD --	K28.2	00 1111 0101 Reserved*
778	92	\	5C	RD +	K28.2	11 0000 1010
277	93	]	5D	RD +	D29.2	01 0001 0101
741	93	]	5D	RD--	D29.2	10 1110 0101
485	94	^	5E	RD--	D30.2	01 1110 0101

533	94	^	5E	RD +	D30.2	10 0001 0101	
325	95	_	5F	RD +	D31.2	01 0100 0101	
693	95	_	5F	RD--	D31.2	10 1011 0101	
339	106	j	6A	RD +	D10.3	01 0101 0011	
348	106	j	6A	RD--	D10.3	01 0101 1100	
835	107	k	6B	RD +	D11.3	11 0100 0011	
844	107	k	6B	RD--	D11.3	11 0100 1100	
211	108	l	6C	RD +	D12.3	00 1101 0011	
220	108	l	6C	RD--	D12.3	00 1101 1100	
707	109	m	6D	RD +	D13.3	10 1100 0011	
716	109	m	6D	RD--	D13.3	10 1100 1100	
451	110	n	6E	RD +	D14.3	01 1100 0011	
460	110	n	6E	RD--	D14.3	01 1100 1100	
371	111	o	6F	RD--	D15.3	01 0111 0011	
652	111	o	6F	RD +	D15.3	10 1000 1100	
355	122	z	7A	RD +	D26.3	01 0110 0011	
364	122	z	7A	RD--	D26.3	01 0110 1100	
156	123	{	7B	RD +	D27.3	00 1001 1100	
867	123	{	7B	RD--	D27.3	11 0110 0011	
227	124	|	7C	RD +	D28.3	00 1110 0011	
236	124	|	7C	RD--	D28.3	00 1110 1100	
243	124	|	7C	RD --	K28.3	00 1111 0011	Reserved*
780	124	|	7C	RD +	K28.3	11 0000 1100	
284	125	}	7D	RD +	D29.3	01 0001 1100	
739	125	}	7D	RD--	D29.3	10 1110 0011	
483	126	~	7E	RD--	D30.3	01 1110 0011	
540	126	~	7E	RD +	D30.3	10 0001 1100	
332	127	DELETE	7F	RD +	D31.3	01 0100 1100	
691	127	DELETE	7F	RD--	D31.3	10 1011 0011	
338	138	Š	8A	RD +	D10.4	01 0101 0010	
349	138	Š	8A	RD--	D10.4	01 0101 1101	
834	139	‹	8B	RD +	D11.4	11 0100 0010	
845	139	‹	8B	RD--	D11.4	11 0100 1101	
210	140	Œ	8C	RD +	D12.4	00 1101 0010	
221	140	Œ	8C	RD--	D12.4	00 1101 1101	
706	141	_	8D	RD +	D13.4	10 1100 0010	
717	141	_	8D	RD--	D13.4	10 1100 1101	
450	142	_	8E	RD +	D14.4	01 1100 0010	
461	142	_	8E	RD--	D14.4	01 1100 1101	
370	143	_	8F	RD--	D15.4	01 0111 0010	
653	143	_	8F	RD +	D15.4	10 1000 1101	
354	154	š	9A	RD +	D26.4	01 0110 0010	
365	154	š	9A	RD--	D26.4	01 0110 1101	
157	155	›	9B	RD +	D27.4	00 1001 1101	
866	155	›	9B	RD--	D27.4	11 0110 0010	
226	156	œ	9C	RD +	D28.4	00 1110 0010	
237	156	œ	9C	RD--	D28.4	00 1110 1101	
242	156	œ	9C	RD --	K28.4	00 1111 0010	Reserved*
781	156	œ	9C	RD +	K28.4	11 0000 1101	
285	157	_	9D	RD +	D29.4	01 0001 1101	
738	157	_	9D	RD--	D29.4	10 1110 0010	
482	158	_	9E	RD--	D30.4	01 1110 0010	
541	158	_	9E	RD +	D30.4	10 0001 1101	
333	159	Ÿ	9F	RD +	D31.4	01 0100 1101	
690	159	Ÿ	9F	RD--	D31.4	10 1011 0010	
394	160		A0	RD +	D0.5	01 1000 1010	
634	160		A0	RD--	D0.5	10 0111 1010	
474	161	¡	A1	RD--	D1.5	01 1101 1010	
554	161	¡	A1	RD +	D1.5	10 0010 1010	
298	162	¢	A2	RD +	D2.5	01 0010 1010	
730	162	¢	A2	RD--	D2.5	10 1101 1010	
794	163	£	A3	RD+/--	D3.5	11 0001 1010	
170	164	¤	A4	RD +	D4.5	00 1010 1010	
858	164	¤	A4	RD--	D4.5	11 0101 1010	
666	165	¥	A5	RD+/--	D5.5	10 1001 1010	
410	166	¦	A6	RD+/--	D6.5	01 1001 1010	
122	167	§	A7	RD +	D7.5	00 0111 1010	
906	167	§	A7	RD--	D7.5	11 1000 1010	
106	168	¨	A8	RD +	D8.5	00 0110 1010	
922	168	¨	A8	RD--	D8.5	11 1001 1010	
602	169	©	A9	RD+/--	D9.5	10 0101 1010	
346	170	ª	AA	RD+/--	D10.5	01 0101 1010	
842	171	«	AB	RD+/--	D11.5	11 0100 1010	
218	172	¬	AC	RD+/--	D12.5	00 1101 1010	
714	173	-	AD	RD+/--	D13.5	10 1100 1010	
458	174	®	AE	RD+/--	D14.5	01 1100 1010	
378	175	¯	AF	RD--	D15.5	01 0111 1010	
650	175	¯	AF	RD +	D15.5	10 1000 1010	
442	176	°	B0	RD--	D16.5	01 1011 1010	
586	176	°	B0	RD +	D16.5	10 0100 1010	
570	177	±	B1	RD+/--	D17.5	10 0011 1010	
314	178	²	B2	RD+/--	D18.5	01 0011 1010	
810	179	³	B3	RD+/--	D19.5	11 0010 1010	
186	180	´	B4	RD+/--	D20.5	00 1011 1010	
682	181	µ	B5	RD+/--	D21.5	10 1010 1010	
426	182	¶	B6	RD+/--	D22.5	01 1010 1010	
90	183	·	B7	RD +	D23.5	00 0101 1010	
938	183	·	B7	RD--	D23.5	11 1010 1010	
202	184	¸	B8	RD +	D24.5	00 1100 1010	
826	184	¸	B8	RD--	D24.5	11 0011 1010	
618	185	¹	B9	RD+/--	D25.5	10 0110 1010	
362	186	º	BA	RD+/--	D26.5	01 0110 1010	
154	187	»	BB	RD +	D27.5	00 1001 1010	
874	187	»	BB	RD--	D27.5	11 0110 1010	
234	188	¼	BC	RD+/--	D28.5	00 1110 1010	
250	188	¼	BC	RD --	K28.5	00 1111 1010	Sync
773	188	¼	BC	RD +	K28.5	11 0000 0101	(Not Used)
282	189	½	BD	RD +	D29.5	01 0001 1010	
746	189	½	BD	RD--	D29.5	10 1110 1010	
490	190	¾	BE	RD--	D30.5	01 1110 1010	
538	190	¾	BE	RD +	D30.5	10 0001 1010	
330	191	¿	BF	RD +	D31.5	01 0100 1010	
698	191	¿	BF	RD--	D31.5	10 1011 1010	
390	192	À	C0	RD +	D0.6	01 1000 0110	
630	192	À	C0	RD--	D0.6	10 0111 0110	
470	193	Á	C1	RD--	D1.6	01 1101 0110	
550	193	Á	C1	RD +	D1.6	10 0010 0110	
294	194	Â	C2	RD +	D2.6	01 0010 0110	
726	194	Â	C2	RD--	D2.6	10 1101 0110	
790	195	Ã	C3	RD+/--	D3.6	11 0001 0110	
166	196	Ä	C4	RD +	D4.6	00 1010 0110	
854	196	Ä	C4	RD--	D4.6	11 0101 0110	
662	197	Å	C5	RD+/--	D5.6	10 1001 0110	
406	198	Æ	C6	RD+/--	D6.6	01 1001 0110	
118	199	Ç	C7	RD +	D7.6	00 0111 0110	
902	199	Ç	C7	RD--	D7.6	11 1000 0110	
102	200	È	C8	RD +	D8.6	00 0110 0110	
918	200	È	C8	RD--	D8.6	11 1001 0110	
598	201	É	C9	RD+/--	D9.6	10 0101 0110	
342	202	Ê	CA	RD+/--	D10.6	01 0101 0110	
838	203	Ë	CB	RD+/--	D11.6	11 0100 0110	
214	204	Ì	CC	RD+/--	D12.6	00 1101 0110	
710	205	Í	CD	RD+/--	D13.6	10 1100 0110	
454	206	Î	CE	RD+/--	D14.6	01 1100 0110	
374	207	Ï	CF	RD--	D15.6	01 0111 0110	
646	207	Ï	CF	RD +	D15.6	10 1000 0110	
438	208	Đ	D0	RD--	D16.6	01 1011 0110	
582	208	Đ	D0	RD +	D16.6	10 0100 0110	

566	209	Ñ	D1	RD+/--	D17.6	10 0011 0110	
310	210	Ò	D2	RD+/--	D18.6	01 0011 0110	
806	211	Ó	D3	RD+/--	D19.6	11 0010 0110	
182	212	Ô	D4	RD+/--	D20.6	00 1011 0110	
678	213	Õ	D5	RD+/--	D21.6	10 1010 0110	
422	214	Ö	D6	RD+/--	D22.6	01 1010 0110	
86	215	×	D7	RD +	D23.6	00 0101 0110	
934	215	×	D7	RD--	D23.6	11 1010 0110	
198	216	Ø	D8	RD +	D24.6	00 1100 0110	
822	216	Ø	D8	RD--	D24.6	11 0011 0110	
614	217	Ù	D9	RD+/--	D25.6	10 0110 0110	
358	218	Ú	DA	RD+/--	D26.6	01 0110 0110	
150	219	Û	DB	RD +	D27.6	00 1001 0110	
870	219	Û	DB	RD--	D27.6	11 0110 0110	
230	220	Ü	DC	RD+/--	D28.6	00 1110 0110	
246	220	Ü	DC	RD --	K28.6	00 1111 0110	Reserved*
777	220	Ü	DC	RD +	K28.6	11 0000 1001	
278	221	Ý	DD	RD +	D29.6	01 0001 0110	
742	221	Ý	DD	RD--	D29.6	10 1110 0110	
486	222	Þ	DE	RD--	D30.6	01 1110 0110	
534	222	Þ	DE	RD +	D30.6	10 0001 0110	
326	223	ß	DF	RD +	D31.6	01 0100 0110	
694	223	ß	DF	RD--	D31.6	10 1011 0110	
398	224	à	E0	RD +	D0.7	01 1000 1110	
625	224	à	E0	RD--	D0.7	10 0111 0001	
465	225	á	E1	RD--	D1.7	01 1101 0001	
558	225	á	E1	RD +	D1.7	10 0010 1110	
302	226	â	E2	RD +	D2.7	01 0010 1110	
721	226	â	E2	RD--	D2.7	10 1101 0001	
785	227	ã	E3	RD +	D3.7	11 0001 0001	
798	227	ã	E3	RD--	D3.7	11 0001 1110	
174	228	ä	E4	RD +	D4.7	00 1010 1110	
849	228	ä	E4	RD--	D4.7	11 0101 0001	
657	229	å	E5	RD +	D5.7	10 1001 0001	
670	229	å	E5	RD--	D5.7	10 1001 1110	
401	230	æ	E6	RD +	D6.7	01 1001 0001	
414	230	æ	E6	RD--	D6.7	01 1001 1110	
113	231	ç	E7	RD +	D7.7	00 0111 0001	
910	231	ç	E7	RD--	D7.7	11 1000 1110	
110	232	è	E8	RD +	D8.7	00 0110 1110	
913	232	è	E8	RD--	D8.7	11 1001 0001	
593	233	é	E9	RD +	D9.7	10 0101 0001	
606	233	é	E9	RD--	D9.7	10 0101 1110	
337	234	ê	EA	RD +	D10.7	01 0101 0001	
350	234	ê	EA	RD--	D10.7	01 0101 1110	
840	235	ë	EB	RD +	D11.7	11 0100 1000	
846	235	ë	EB	RD--	D11.7	11 0100 1110	
209	236	ì	EC	RD +	D12.7	00 1101 0001	
222	236	ì	EC	RD--	D12.7	00 1101 1110	
712	237	í	ED	RD +	D13.7	10 1100 1000	
718	237	í	ED	RD--	D13.7	10 1100 1110	
456	238	î	EE	RD +	D14.7	01 1100 1000	
462	238	î	EE	RD--	D14.7	01 1100 1110	
369	239	ï	EF	RD--	D15.7	01 0111 0001	
654	239	ï	EF	RD +	D15.7	10 1000 1110	
433	240	ð	F0	RD--	D16.7	01 1011 0001	
590	240	ð	F0	RD +	D16.7	10 0100 1110	
561	241	ñ	F1	RD +	D17.7	10 0011 0001	
567	241	ñ	F1	RD--	D17.7	10 0011 0111	
305	242	ò	F2	RD +	D18.7	01 0011 0001	
311	242	ò	F2	RD--	D18.7	01 0011 0111	
801	243	ó	F3	RD +	D19.7	11 0010 0001	
814	243	ó	F3	RD--	D19.7	11 0010 1110	
177	244	ô	F4	RD +	D20.7	00 1011 0001	
183	244	ô	F4	RD--	D20.7	00 1011 0111	
673	245	õ	F5	RD +	D21.7	10 1010 0001	
686	245	õ	F5	RD--	D21.7	10 1010 1110	
417	246	ö	F6	RD +	D22.7	01 1010 0001	
430	246	ö	F6	RD--	D22.7	01 1010 1110	
87	247	÷	F7	RD +	K23.7	00 0101 0111	
94	247	÷	F7	RD +	D23.7	00 0101 1110	
929	247	÷	F7	RD--	D23.7	11 1010 0001	
936	247	÷	F7	RD --	K23.7	11 1010 1000	Reserved*
206	248	ø	F8	RD +	D24.7	00 1100 1110	
817	248	ø	F8	RD--	D24.7	11 0011 0001	
609	249	ù	F9	RD +	D25.7	10 0110 0001	
622	249	ù	F9	RD--	D25.7	10 0110 1110	
353	250	ú	FA	RD +	D26.7	01 0110 0001	
366	250	ú	FA	RD--	D26.7	01 0110 1110	
151	251	û	FB	RD +	K27.7	00 1001 0111	
158	251	û	FB	RD +	D27.7	00 1001 1110	
865	251	û	FB	RD--	D27.7	11 0110 0001	
872	251	û	FB	RD --	K27.7	11 0110 1000	Reserved*
225	252	ü	FC	RD +	D28.7	00 1110 0001	
238	252	ü	FC	RD--	D28.7	00 1110 1110	
248	252	ü	FC	RD --	K28.7	00 1111 1000	Test
775	252	ü	FC	RD +	K28.7	11 0000 0111	
279	253	ý	FD	RD +	K29.7	01 0001 0111	
286	253	ý	FD	RD +	D29.7	01 0001 1110	
737	253	ý	FD	RD--	D29.7	10 1110 0001	
744	253	ý	FD	RD --	K29.7	10 1110 1000	Reserved*
481	254	þ	FE	RD--	D30.7	01 1110 0001	
488	254	þ	FE	RD --	K30.7	01 1110 1000	Reserved*
535	254	þ	FE	RD +	K30.7	10 0001 0111	
542	254	þ	FE	RD +	D30.7	10 0001 1110	
334	255	ÿ	FF	RD +	D31.7	01 0100 1110	
689	255	ÿ	FF	RD--	D31.7	10 1011 0001	

The following table lists:

Legal 10-bit Values Sorted by K/D Code

10B Dec	8B Dec	ASCII+	HEX	Previous Disparity	Data Byte FC Name	10 B	COMMENT
395	0	NUL	00	RD +	D0.0	01 1000 1011	
628	0	NUL	00	RD--	D0.0	10 0111 0100	
393	32	SPACE	20	RD +	D0.1	01 1000 1001	
633	32	SPACE	20	RD--	D0.1	10 0111 1001	
389	64	@	40	RD +	D0.2	01 1000 0101	
629	64	@	40	RD--	D0.2	10 0111 0101	
396	96	`	60	RD +	D0.3	01 1000 1100	
627	96	`	60	RD--	D0.3	10 0111 0011	
397	128	_	80	RD +	D0.4	01 1000 1101	
626	128	_	80	RD--	D0.4	10 0111 0010	
394	160		A0	RD +	D0.5	01 1000 1010	
634	160		A0	RD--	D0.5	10 0111 1010	
390	192	À	C0	RD +	D0.6	01 1000 0110	
630	192	À	C0	RD--	D0.6	10 0111 0110	
398	224	à	E0	RD +	D0.7	01 1000 1110	
625	224	à	E0	RD--	D0.7	10 0111 0001	
468	1	SOH	01	RD--	D1.0	01 1101 0100	
555	1	SOH	01	RD +	D1.0	10 0010 1011	
473	33	!	21	RD--	D1.1	01 1101 1001	
553	33	!	21	RD +	D1.1	10 0010 1001	
469	65	A	41	RD--	D1.2	01 1101 0101	
549	65	A	41	RD +	D1.2	10 0010 0101	
467	97	a	61	RD--	D1.3	01 1101 0011	
556	97	a	61	RD +	D1.3	10 0010 1100	
466	129	_	81	RD--	D1.4	01 1101 0010	
557	129	_	81	RD +	D1.4	10 0010 1101	
474	161	¡	A1	RD--	D1.5	01 1101 1010	
554	161	¡	A1	RD +	D1.5	10 0010 1010	
470	193	Á	C1	RD--	D1.6	01 1101 0110	
550	193	Á	C1	RD +	D1.6	10 0010 0110	
465	225	á	E1	RD--	D1.7	01 1101 0001	
558	225	á	E1	RD +	D1.7	10 0010 1110	
340	10	LF	0A	RD +	D10.0	01 0101 0100	
347	10	LF	0A	RD--	D10.0	01 0101 1011	
345	42	*	2A	RD+/--	D10.1	01 0101 1001	
341	74	J	4A	RD+/--	D10.2	01 0101 0101	
339	106	j	6A	RD +	D10.3	01 0101 0011	
348	106	j	6A	RD--	D10.3	01 0101 1100	
338	138	Š	8A	RD +	D10.4	01 0101 0010	
349	138	Š	8A	RD--	D10.4	01 0101 1101	
346	170	ª	AA	RD+/--	D10.5	01 0101 1010	
342	202	Ê	CA	RD+/--	D10.6	01 0101 0110	
337	234	ê	EA	RD +	D10.7	01 0101 0001	
350	234	ê	EA	RD--	D10.7	01 0101 1110	
836	11	VT	0B	RD +	D11.0	11 0100 0100	
843	11	VT	0B	RD--	D11.0	11 0100 1011	
841	43	+	2B	RD+/--	D11.1	11 0100 1001	
837	75	K	4B	RD+/--	D11.2	11 0100 0101	
835	107	k	6B	RD +	D11.3	11 0100 0011	
844	107	k	6B	RD--	D11.3	11 0100 1100	
834	139	‹	8B	RD +	D11.4	11 0100 0010	
845	139	‹	8B	RD--	D11.4	11 0100 1101	
842	171	«	AB	RD+/--	D11.5	11 0100 1010	
838	203	Ë	CB	RD+/--	D11.6	11 0100 0110	
840	235	ë	EB	RD +	D11.7	11 0100 1000	
846	235	ë	EB	RD--	D11.7	11 0100 1110	
212	12	FF	0C	RD +	D12.0	00 1101 0100	
219	12	FF	0C	RD--	D12.0	00 1101 1011	
217	44	,	2C	RD+/--	D12.1	00 1101 1001	
213	76	L	4C	RD+/--	D12.2	00 1101 0101	
211	108	l	6C	RD +	D12.3	00 1101 0011	
220	108	l	6C	RD--	D12.3	00 1101 1100	
210	140	Œ	8C	RD +	D12.4	00 1101 0010	
221	140	Œ	8C	RD--	D12.4	00 1101 1101	
218	172	¬	AC	RD+/--	D12.5	00 1101 1010	
214	204	Ì	CC	RD+/--	D12.6	00 1101 0110	
209	236	ì	EC	RD +	D12.7	00 1101 0001	
222	236	ì	EC	RD--	D12.7	00 1101 1110	
708	13	CR	0D	RD +	D13.0	10 1100 0100	
715	13	CR	0D	RD--	D13.0	10 1100 1011	
713	45	-	2D	RD+/--	D13.1	10 1100 1001	
709	77	M	4D	RD+/--	D13.2	10 1100 0101	
707	109	m	6D	RD +	D13.3	10 1100 0011	
716	109	m	6D	RD--	D13.3	10 1100 1100	
706	141	_	8D	RD +	D13.4	10 1100 0010	
717	141	_	8D	RD--	D13.4	10 1100 1101	
714	173	-	AD	RD+/--	D13.5	10 1100 1010	
710	205	Í	CD	RD+/--	D13.6	10 1100 0110	
712	237	í	ED	RD +	D13.7	10 1100 1000	
718	237	í	ED	RD--	D13.7	10 1100 1110	
452	14	SO	0E	RD +	D14.0	01 1100 0100	
459	14	SO	0E	RD--	D14.0	01 1100 1011	
457	46	.	2E	RD+/--	D14.1	01 1100 1001	
453	78	N	4E	RD+/--	D14.2	01 1100 0101	
451	110	n	6E	RD +	D14.3	01 1100 0011	
460	110	n	6E	RD--	D14.3	01 1100 1100	
450	142	_	8E	RD +	D14.4	01 1100 0010	
461	142	_	8E	RD--	D14.4	01 1100 1101	
458	174	®	AE	RD+/--	D14.5	01 1100 1010	
454	206	Î	CE	RD+/--	D14.6	01 1100 0110	
456	238	î	EE	RD +	D14.7	01 1100 1000	
462	238	î	EE	RD--	D14.7	01 1100 1110	
372	15	SI	0F	RD--	D15.0	01 0111 0100	
651	15	SI	0F	RD +	D15.0	10 1000 1011	
377	47	/	2F	RD--	D15.1	01 0111 1001	
649	47	/	2F	RD +	D15.1	10 1000 1001	
373	79	O	4F	RD--	D15.2	01 0111 0101	
645	79	O	4F	RD +	D15.2	10 1000 0101	
371	111	o	6F	RD--	D15.3	01 0111 0011	
652	111	o	6F	RD +	D15.3	10 1000 1100	
370	143	_	8F	RD--	D15.4	01 0111 0010	
653	143	_	8F	RD +	D15.4	10 1000 1101	
378	175	¯	AF	RD--	D15.5	01 0111 1010	
650	175	¯	AF	RD +	D15.5	10 1000 1010	
374	207	Ï	CF	RD--	D15.6	01 0111 0110	
646	207	Ï	CF	RD +	D15.6	10 1000 0110	
369	239	ï	EF	RD--	D15.7	01 0111 0001	
654	239	ï	EF	RD +	D15.7	10 1000 1110	
436	16	DLE	10	RD--	D16.0	01 1011 0100	
587	16	DLE	10	RD +	D16.0	10 0100 1011	
441	48	0	30	RD--	D16.1	01 1011 1001	
585	48	0	30	RD +	D16.1	10 0100 1001	
437	80	P	50	RD--	D16.2	01 1011 0101	
581	80	P	50	RD +	D16.2	10 0100 0101	
435	112	p	70	RD--	D16.3	01 1011 0011	
588	112	p	70	RD +	D16.3	10 0100 1100	
434	144	_	90	RD--	D16.4	01 1011 0010	
589	144	_	90	RD +	D16.4	10 0100 1101	
442	176	°	B0	RD--	D16.5	01 1011 1010	
586	176	°	B0	RD +	D16.5	10 0100 1010	
438	208	Ð	D0	RD--	D16.6	01 1011 0110	
582	208	Ð	D0	RD +	D16.6	10 0100 0110	
433	240	ð	F0	RD--	D16.7	01 1011 0001	
590	240	ð	F0	RD +	D16.7	10 0100 1110	
564	17	DC1	11	RD +	D17.0	10 0011 0100	
571	17	DC1	11	RD--	D17.0	10 0011 1011	
569	49	1	31	RD+/--	D17.1	10 0011 1001	
565	81	Q	51	RD+/--	D17.2	10 0011 0101	
563	113	q	71	RD +	D17.3	10 0011 0011	
572	113	q	71	RD--	D17.3	10 0011 1100	
562	145	‘	91	RD +	D17.4	10 0011 0010	

573	145	‘	91	RD--	D17.4	10 0011 1101		419	118	v	76	RD +	D22.3	01 1010 0011
570	177	±	B1	RD+/--	D17.5	10 0011 1010		428	118	v	76	RD--	D22.3	01 1010 1100
566	209	Ñ	D1	RD+/--	D17.6	10 0011 0110		418	150	–	96	RD +	D22.4	01 1010 0010
561	241	ñ	F1	RD +	D17.7	10 0011 0001		429	150	–	96	RD--	D22.4	01 1010 1101
567	241	ñ	F1	RD--	D17.7	10 0011 0111		426	182	¶	B6	RD+/--	D22.5	01 1010 1010
308	18	DC2	12	RD +	D18.0	01 0011 0100		422	214	Ö	D6	RD+/--	D22.6	01 1010 0110
315	18	DC2	12	RD--	D18.0	01 0011 1011		417	246	ö	F6	RD +	D22.7	01 1010 0001
313	50	2	32	RD+/--	D18.1	01 0011 1001		430	246	ö	F6	RD--	D22.7	01 1010 1110
309	82	R	52	RD+/--	D18.2	01 0011 0101		91	23	ETB	17	RD +	D23.0	00 0101 1011
307	114	r	72	RD +	D18.3	01 0011 0011		932	23	ETB	17	RD--	D23.0	11 1010 0100
316	114	r	72	RD--	D18.3	01 0011 1100		89	55	7	37	RD +	D23.1	00 0101 1001
306	146	’	92	RD +	D18.4	01 0011 0010		937	55	7	37	RD--	D23.1	11 1010 1001
317	146	’	92	RD--	D18.4	01 0011 1101		85	87	W	57	RD +	D23.2	00 0101 0101
314	178	²	B2	RD+/--	D18.5	01 0011 1010		933	87	W	57	RD--	D23.2	11 1010 0101
310	210	Ò	D2	RD+/--	D18.6	01 0011 0110		92	119	w	77	RD +	D23.3	00 0101 1100
305	242	ò	F2	RD +	D18.7	01 0011 0001		931	119	w	77	RD--	D23.3	11 1010 0011
311	242	ò	F2	RD--	D18.7	01 0011 0111		93	151	—	97	RD +	D23.4	00 0101 1101
804	19	DC3	13	RD +	D19.0	11 0010 0100		930	151	—	97	RD--	D23.4	11 1010 0010
811	19	DC3	13	RD--	D19.0	11 0010 1011		90	183	·	B7	RD +	D23.5	00 0101 1010
809	51	3	33	RD+/--	D19.1	11 0010 1001		938	183	·	B7	RD--	D23.5	11 1010 1010
805	83	S	53	RD+/--	D19.2	11 0010 0101		86	215	×	D7	RD +	D23.6	00 0101 0110
803	115	s	73	RD +	D19.3	11 0010 0011		934	215	×	D7	RD--	D23.6	11 1010 0110
812	115	s	73	RD--	D19.3	11 0010 1100		94	247	÷	F7	RD +	D23.7	00 0101 1110
802	147	“	93	RD +	D19.4	11 0010 0010		929	247	÷	F7	RD--	D23.7	11 1010 0001
813	147	“	93	RD--	D19.4	11 0010 1101		203	24	CAN	18	RD +	D24.0	00 1100 1011
810	179	³	B3	RD+/--	D19.5	11 0010 1010		820	24	CAN	18	RD--	D24.0	11 0011 0100
806	211	Ó	D3	RD+/--	D19.6	11 0010 0110		201	56	8	38	RD +	D24.1	00 1100 1001
801	243	ó	F3	RD +	D19.7	11 0010 0001		825	56	8	38	RD--	D24.1	11 0011 1001
814	243	ó	F3	RD--	D19.7	11 0010 1110		197	88	X	58	RD +	D24.2	00 1100 0101
299	2	STX	02	RD +	D2.0	01 0010 1011		821	88	X	58	RD--	D24.2	11 0011 0101
724	2	STX	02	RD--	D2.0	10 1101 0100		204	120	x	78	RD +	D24.3	00 1100 1100
297	34	"	22	RD +	D2.1	01 0010 1001		819	120	x	78	RD--	D24.3	11 0011 0011
729	34	"	22	RD--	D2.1	10 1101 1001		205	152	˜	98	RD +	D24.4	00 1100 1101
293	66	B	42	RD +	D2.2	01 0010 0101		818	152	˜	98	RD--	D24.4	11 0011 0010
725	66	B	42	RD--	D2.2	10 1101 0101		202	184	¸	B8	RD +	D24.5	00 1100 1010
300	98	b	62	RD +	D2.3	01 0010 1100		826	184	¸	B8	RD--	D24.5	11 0011 1010
723	98	b	62	RD--	D2.3	10 1101 0011		198	216	Ø	D8	RD +	D24.6	00 1100 0110
301	130	‚	82	RD +	D2.4	01 0010 1101		822	216	Ø	D8	RD--	D24.6	11 0011 0110
722	130	‚	82	RD--	D2.4	10 1101 0010		206	248	ø	F8	RD +	D24.7	00 1100 1110
298	162	¢	A2	RD +	D2.5	01 0010 1010		817	248	ø	F8	RD--	D24.7	11 0011 0001
730	162	¢	A2	RD--	D2.5	10 1101 1010		612	25	EM	19	RD +	D25.0	10 0110 0100
294	194	Â	C2	RD +	D2.6	01 0010 0110		619	25	EM	19	RD--	D25.0	10 0110 1011
726	194	Â	C2	RD--	D2.6	10 1101 0110		617	57	9	39	RD+/--	D25.1	10 0110 1001
302	226	â	E2	RD +	D2.7	01 0010 1110		613	89	Y	59	RD+/--	D25.2	10 0110 0101
721	226	â	E2	RD--	D2.7	10 1101 0001		611	121	y	79	RD +	D25.3	10 0110 0011
180	20	DC4	14	RD +	D20.0	00 1011 0100		620	121	y	79	RD--	D25.3	10 0110 1100
187	20	DC4	14	RD--	D20.0	00 1011 1011		610	153	™	99	RD +	D25.4	10 0110 0010
185	52	4	34	RD+/--	D20.1	00 1011 1001		621	153	™	99	RD--	D25.4	10 0110 1101
181	84	T	54	RD+/--	D20.2	00 1011 0101		618	185	¹	B9	RD+/--	D25.5	10 0110 1010
179	116	t	74	RD +	D20.3	00 1011 0011		614	217	Ù	D9	RD+/--	D25.6	10 0110 0110
188	116	t	74	RD--	D20.3	00 1011 1100		609	249	ù	F9	RD +	D25.7	10 0110 0001
178	148	”	94	RD +	D20.4	00 1011 0010		622	249	ù	F9	RD--	D25.7	10 0110 1110
189	148	”	94	RD--	D20.4	00 1011 1101		356	26	SUB	1A	RD +	D26.0	01 0110 0100
186	180	´	B4	RD+/--	D20.5	00 1011 1010		363	26	SUB	1A	RD--	D26.0	01 0110 1011
182	212	Ô	D4	RD+/--	D20.6	00 1011 0110		361	58	:	3A	RD+/--	D26.1	01 0110 1001
177	244	ô	F4	RD +	D20.7	00 1011 0001		357	90	Z	5A	RD+/--	D26.2	01 0110 0101
183	244	ô	F4	RD--	D20.7	00 1011 0111		355	122	z	7A	RD +	D26.3	01 0110 0011
676	21	NAK	15	RD +	D21.0	10 1010 0100		364	122	z	7A	RD--	D26.3	01 0110 1100
683	21	NAK	15	RD--	D21.0	10 1010 1011		354	154	š	9A	RD +	D26.4	01 0110 0010
681	53	5	35	RD+/--	D21.1	10 1010 1001		365	154	š	9A	RD--	D26.4	01 0110 1101
677	85	U	55	RD+/--	D21.2	10 1010 0101		362	186	º	BA	RD+/--	D26.5	01 0110 1010
675	117	u	75	RD +	D21.3	10 1010 0011		358	218	Ú	DA	RD+/--	D26.6	01 0110 0110
684	117	u	75	RD--	D21.3	10 1010 1100		353	250	ú	FA	RD +	D26.7	01 0110 0001
674	149	•	95	RD +	D21.4	10 1010 0010		366	250	ú	FA	RD--	D26.7	01 0110 1110
685	149	•	95	RD--	D21.4	10 1010 1101		155	27	ESC	1B	RD +	D27.0	00 1001 1011
682	181	µ	B5	RD+/--	D21.5	10 1010 1010		868	27	ESC	1B	RD--	D27.0	11 0110 0100
678	213	Õ	D5	RD+/--	D21.6	10 1010 0110		153	59	;	3B	RD +	D27.1	00 1001 1001
673	245	õ	F5	RD +	D21.7	10 1010 0001		873	59	;	3B	RD--	D27.1	11 0110 1001
686	245	õ	F5	RD--	D21.7	10 1010 1110		149	91	[	5B	RD +	D27.2	00 1001 0101
420	22	SYN	16	RD +	D22.0	01 1010 0100		869	91	[	5B	RD--	D27.2	11 0110 0101
427	22	SYN	16	RD--	D22.0	01 1010 1011		156	123	{	7B	RD +	D27.3	00 1001 1100
425	54	6	36	RD+/--	D22.1	01 1010 1001		867	123	{	7B	RD--	D27.3	11 0110 0011
421	86	V	56	RD+/--	D22.2	01 1010 0101		157	155	›	9B	RD +	D27.4	00 1001 1101

866	155	›	9B	RD--	D27.4	11 0110 0010
154	187	»	BB	RD +	D27.5	00 1001 1010
874	187	»	BB	RD--	D27.5	11 0110 1010
150	219	Û	DB	RD +	D27.6	00 1001 0110
870	219	Û	DB	RD--	D27.6	11 0110 0110
158	251	û	FB	RD +	D27.7	00 1001 1110
865	251	û	FB	RD--	D27.7	11 0110 0001
228	28	FS	1C	RD +	D28.0	00 1110 0100
235	28	FS	1C	RD--	D28.0	00 1110 1011
233	60	<	3C	RD+/--	D28.1	00 1110 1001
229	92	\	5C	RD+/--	D28.2	00 1110 0101
227	124	|	7C	RD +	D28.3	00 1110 0011
236	124	|	7C	RD--	D28.3	00 1110 1100
226	156	œ	9C	RD +	D28.4	00 1110 0010
237	156	œ	9C	RD--	D28.4	00 1110 1101
234	188	¼	BC	RD+/--	D28.5	00 1110 1010
230	220	Ü	DC	RD+/--	D28.6	00 1110 0110
225	252	ü	FC	RD +	D28.7	00 1110 0001
238	252	ü	FC	RD--	D28.7	00 1110 1110
283	29	GS	1D	RD +	D29.0	01 0001 1011
740	29	GS	1D	RD--	D29.0	10 1110 0100
281	61	=	3D	RD +	D29.1	01 0001 1001
745	61	=	3D	RD--	D29.1	10 1110 1001
277	93	]	5D	RD +	D29.2	01 0001 0101
741	93	]	5D	RD--	D29.2	10 1110 0101
284	125	}	7D	RD +	D29.3	01 0001 1100
739	125	}	7D	RD--	D29.3	10 1110 0011
285	157	_	9D	RD +	D29.4	01 0001 1101
738	157	_	9D	RD--	D29.4	10 1110 0010
282	189	½	BD	RD +	D29.5	01 0001 1010
746	189	½	BD	RD--	D29.5	10 1110 1010
278	221	Ý	DD	RD +	D29.6	01 0001 0110
742	221	Ý	DD	RD--	D29.6	10 1110 0110
286	253	ý	FD	RD +	D29.7	01 0001 1110
737	253	ý	FD	RD--	D29.7	10 1110 0001
788	3	ETX	03	RD +	D3.0	11 0001 0100
795	3	ETX	03	RD--	D3.0	11 0001 1011
793	35	#	23	RD+/--	D3.1	11 0001 1001
789	67	C	43	RD+/--	D3.2	11 0001 0101
787	99	c	63	RD +	D3.3	11 0001 0011
796	99	c	63	RD--	D3.3	11 0001 1100
786	131	ƒ	83	RD +	D3.4	11 0001 0010
797	131	ƒ	83	RD--	D3.4	11 0001 1101
794	163	£	A3	RD+/--	D3.5	11 0001 1010
790	195	Ã	C3	RD+/--	D3.6	11 0001 0110
785	227	ã	E3	RD +	D3.7	11 0001 0001
798	227	ã	E3	RD--	D3.7	11 0001 1110
484	30	RS	1E	RD--	D30.0	01 1110 0100
539	30	RS	1E	RD +	D30.0	10 0001 1011
489	62	>	3E	RD--	D30.1	01 1110 1001
537	62	>	3E	RD +	D30.1	10 0001 1001
485	94	^	5E	RD--	D30.2	01 1110 0101
533	94	^	5E	RD +	D30.2	10 0001 0101
483	126	~	7E	RD--	D30.3	01 1110 0011
540	126	~	7E	RD +	D30.3	10 0001 1100
482	158	_	9E	RD--	D30.4	01 1110 0010
541	158	_	9E	RD +	D30.4	10 0001 1101
490	190	¾	BE	RD--	D30.5	01 1110 1010
538	190	¾	BE	RD +	D30.5	10 0001 1010
486	222	Þ	DE	RD--	D30.6	01 1110 0110
534	222	Þ	DE	RD +	D30.6	10 0001 0110
481	254	þ	FE	RD--	D30.7	01 1110 0001
542	254	þ	FE	RD +	D30.7	10 0001 1110
331	31	US	1F	RD +	D31.0	01 0100 1011
692	31	US	1F	RD--	D31.0	10 1011 0100
329	63	?	3F	RD +	D31.1	01 0100 1001
697	63	?	3F	RD--	D31.1	10 1011 1001
325	95	_	5F	RD +	D31.2	01 0100 0101
693	95	_	5F	RD--	D31.2	10 1011 0101
332	127	DELETE	7F	RD +	D31.3	01 0100 1100
691	127	DELETE	7F	RD--	D31.3	10 1011 0011
333	159	Ÿ	9F	RD +	D31.4	01 0100 1101
690	159	Ÿ	9F	RD--	D31.4	10 1011 0010
330	191	¿	BF	RD +	D31.5	01 0100 1010
698	191	¿	BF	RD--	D31.5	10 1011 1010
326	223	ß	DF	RD +	D31.6	01 0100 0110
694	223	ß	DF	RD--	D31.6	10 1011 0110
334	255	ÿ	FF	RD +	D31.7	01 0100 1110
689	255	ÿ	FF	RD--	D31.7	10 1011 0001
171	4	EOT	04	RD +	D4.0	00 1010 1011
852	4	EOT	04	RD--	D4.0	11 0101 0100
169	36	$	24	RD +	D4.1	00 1010 1001
857	36	$	24	RD--	D4.1	11 0101 1001
165	68	D	44	RD +	D4.2	00 1010 0101
853	68	D	44	RD--	D4.2	11 0101 0101
172	100	d	64	RD +	D4.3	00 1010 1100
851	100	d	64	RD--	D4.3	11 0101 0011
173	132	„	84	RD +	D4.4	00 1010 1101
850	132	„	84	RD--	D4.4	11 0101 0010
170	164	¤	A4	RD +	D4.5	00 1010 1010
858	164	¤	A4	RD--	D4.5	11 0101 1010
166	196	Ä	C4	RD +	D4.6	00 1010 0110
854	196	Ä	C4	RD--	D4.6	11 0101 0110
174	228	ä	E4	RD +	D4.7	00 1010 1110
849	228	ä	E4	RD--	D4.7	11 0101 0001
660	5	ENQ	05	RD +	D5.0	10 1001 0100
667	5	ENQ	05	RD--	D5.0	10 1001 1011
665	37	%	25	RD+/--	D5.1	10 1001 1001
661	69	E	45	RD+/--	D5.2	10 1001 0101
659	101	e	65	RD +	D5.3	10 1001 0011
668	101	e	65	RD--	D5.3	10 1001 1100
658	133	…	85	RD +	D5.4	10 1001 0010
669	133	…	85	RD--	D5.4	10 1001 1101
666	165	¥	A5	RD+/--	D5.5	10 1001 1010
662	197	Å	C5	RD+/--	D5.6	10 1001 0110
657	229	å	E5	RD +	D5.7	10 1001 0001
670	229	å	E5	RD--	D5.7	10 1001 1110
404	6	ACK	06	RD +	D6.0	01 1001 0100
411	6	ACK	06	RD--	D6.0	01 1001 1011
409	38	&	26	RD+/--	D6.1	01 1001 1001
405	70	F	46	RD+/--	D6.2	01 1001 0101
403	102	f	66	RD +	D6.3	01 1001 0011
412	102	f	66	RD--	D6.3	01 1001 1100
402	134	†	86	RD +	D6.4	01 1001 0010
413	134	†	86	RD--	D6.4	01 1001 1101
410	166	¦	A6	RD+/--	D6.5	01 1001 1010
406	198	Æ	C6	RD+/--	D6.6	01 1001 0110
401	230	æ	E6	RD +	D6.7	01 1001 0001
414	230	æ	E6	RD--	D6.7	01 1001 1110
116	7	BEL	07	RD +	D7.0	00 0111 0100
907	7	BEL	07	RD--	D7.0	11 1000 1011
121	39	'	27	RD +	D7.1	00 0111 1001
905	39	'	27	RD--	D7.1	11 1000 1001
117	71	G	47	RD +	D7.2	00 0111 0101
901	71	G	47	RD--	D7.2	11 1000 0101
115	103	g	67	RD +	D7.3	00 0111 0011
908	103	g	67	RD--	D7.3	11 1000 1100
114	135	‡	87	RD +	D7.4	00 0111 0010
909	135	‡	87	RD--	D7.4	11 1000 1101
122	167	§	A7	RD +	D7.5	00 0111 1010
906	167	§	A7	RD--	D7.5	11 1000 1010
118	199	Ç	C7	RD +	D7.6	00 0111 0110
902	199	Ç	C7	RD--	D7.6	11 1000 0110
113	231	ç	E7	RD +	D7.7	00 0111 0001
910	231	ç	E7	RD--	D7.7	11 1000 1110
107	8	BS	08	RD +	D8.0	00 0110 1011
916	8	BS	08	RD--	D8.0	11 1001 0100
105	40	(	28	RD +	D8.1	00 0110 1001
921	40	(	28	RD--	D8.1	11 1001 1001
101	72	H	48	RD +	D8.2	00 0110 0101
917	72	H	48	RD--	D8.2	11 1001 0101
108	104	h	68	RD +	D8.3	00 0110 1100
915	104	h	68	RD--	D8.3	11 1001 0011
109	136	ˆ	88	RD +	D8.4	00 0110 1101
914	136	ˆ	88	RD--	D8.4	11 1001 0010
106	168	¨	A8	RD +	D8.5	00 0110 1010

922	168	¨	A8	RD--	D8.5	11 1001 1010	
102	200	È	C8	RD +	D8.6	00 0110 0110	
918	200	È	C8	RD--	D8.6	11 1001 0110	
110	232	è	E8	RD +	D8.7	00 0110 1110	
913	232	è	E8	RD--	D8.7	11 1001 0001	
596	9	HT	09	RD +	D9.0	10 0101 0100	
603	9	HT	09	RD--	D9.0	10 0101 1011	
601	41	)	29	RD+/--	D9.1	10 0101 1001	
597	73	I	49	RD+/--	D9.2	10 0101 0101	
595	105	i	69	RD +	D9.3	10 0101 0011	
604	105	i	69	RD--	D9.3	10 0101 1100	
594	137	‰	89	RD +	D9.4	10 0101 0010	
605	137	‰	89	RD--	D9.4	10 0101 1101	
602	169	©	A9	RD+/--	D9.5	10 0101 1010	
598	201	É	C9	RD+/--	D9.6	10 0101 0110	
593	233	é	E9	RD +	D9.7	10 0101 0001	
606	233	é	E9	RD--	D9.7	10 0101 1110	
87	247	÷	F7	RD +	K23.7	00 0101 0111	
936	247	÷	F7	RD --	K23.7	11 1010 1000	Reserved*
151	251	û	FB	RD +	K27.7	00 1001 0111	
872	251	û	FB	RD --	K27.7	11 0110 1000	Reserved*
244	28	FS	1C	RD --	K28.0	00 1111 0100	Reserved*
779	28	FS	1C	RD +	K28.0	11 0000 1011	
249	60	<	3C	RD --	K28.1	00 1111 1001	Reserved*
774	60	<	3C	RD +	K28.1	11 0000 0110	
245	92	\	5C	RD --	K28.2	00 1111 0101	Reserved*
778	92	\	5C	RD +	K28.2	11 0000 1010	
243	124	|	7C	RD --	K28.3	00 1111 0011	Reserved*
780	124	|	7C	RD +	K28.3	11 0000 1100	
242	156	œ	9C	RD --	K28.4	00 1111 0010	Reserved*
781	156	œ	9C	RD +	K28.4	11 0000 1101	
250	188	¼	BC	RD --	K28.5	00 1111 1010	Sync
773	188	¼	BC	RD +	K28.5	11 0000 0101	(Not Used)
246	220	Ü	DC	RD --	K28.6	00 1111 0110	Reserved*
777	220	Ü	DC	RD +	K28.6	11 0000 1001	
248	252	ü	FC	RD --	K28.7	00 1111 1000	Test
775	252	ü	FC	RD +	K28.7	11 0000 0111	
279	253	ý	FD	RD +	K29.7	01 0001 0111	
744	253	ý	FD	RD --	K29.7	10 1110 1000	Reserved*
488	254	þ	FE	RD --	K30.7	01 1110 1000	Reserved*
535	254	þ	FE	RD +	K30.7	10 0001 0111	

Appendix C

Fibre Channel Legal Arbitrated Loop Physical Addresses

This appendix contains legal (neutral disparity) arbitrated loop physical addresses (APLAs) sorted from highest (at the top) to the lowest (at the bottom) priority.

Loop ID	ALPAA HEX	Name	RD -- Code	RD-/+ Code	Previous Running Disparity RD+ Code
7E	00	D0.0	10 0111 0100		01 1000 1011
7D	01	D1.0	01 1101 0100		10 0010 1011
7C	02	D2.0	10 1101 0100		01 0010 1011
7B	04	D4.0	11 0101 0100		00 1010 1011
7A	08	D8.0	11 1001 0100		00 0110 1011
79	0F	D15.0	01 0111 0100		10 1000 1011
78	10	D16.0	01 1011 0100		10 0100 1011
77	17	D23.0	11 1010 0100		00 0101 1011
76	18	D24.0	11 0011 0100		00 1100 1011
75	1B	D27.0	11 0110 0100		00 1001 1011
74	1D	D29.0	10 1110 0100		01 0001 1011
73	1E	D30.0	01 1110 0100		10 0001 1011
72	1F	D31.0	10 1011 0100		01 0100 1011
71	23	D3.1		11 0001 1001	
70	25	D5.1		10 1001 1001	
6F	26	D6.1		01 1001 1001	
6E	27	D7.1	11 1000 1001		00 0111 1001
6D	29	D9.1		10 0101 1001	
6C	2A	D10.1		01 0101 1001	
6B	2B	D11.1		11 0100 1001	
6A	2C	D12.1		00 1101 1001	
69	2D	D13.1		10 1100 1001	
68	2E	D14.1		01 1100 1001	
67	31	D17.1		10 0011 1001	
66	32	D18.1		01 0011 1001	
65	33	D19.1		11 0010 1001	
64	34	D20.1		00 1011 1001	
63	35	D21.1		10 1010 1001	
62	36	D22.1		01 1010 1001	
61	39	D25.1		10 0110 1001	
60	3A	D26.1		01 0110 1001	
5F	3C	D28.1		00 1110 1001	
5E	43	D3.2		11 0001 0101	
5D	45	D5.2		10 1001 0101	
5C	46	D6.2		01 1001 0101	
5B	47	D7.2	11 1000 0101		00 0111 0101
5A	49	D9.2		10 0101 0101	
59	4A	D10.2		01 0101 0101	
58	4B	D11.2		11 0100 0101	
57	4C	D12.2		00 1101 0101	
56	4D	D13.2		10 1100 0101	
55	4E	D14.2		01 1100 0101	
54	51	D17.2		10 0011 0101	
53	52	D18.2		01 0011 0101	
52	53	D19.2		11 0010 0101	
51	54	D20.2		00 1011 0101	
50	55	D21.2		10 1010 0101	
4F	56	D22.2		01 1010 0101	
4E	59	D25.2		10 0110 0101	
4D	5A	D26.2		01 0110 0101	
4C	5C	D28.2		00 1110 0101	
4B	63	D3.3	11 0001 1100		11 0001 0011
4A	65	D5.3	10 1001 1100		10 1001 0011
49	66	D6.3	01 1001 1100		01 1001 0011
48	67	D7.3	11 1000 1100		00 0111 0011
47	69	D9.3	10 0101 1100		10 0101 0011
46	6A	D10.3	01 0101 1100		01 0101 0011
45	6B	D11.3	11 0100 1100		11 0100 0011
44	6C	D12.3	00 1101 1100		00 1101 0011
43	6D	D13.3	10 1100 1100		10 1100 0011
42	6E	D14.3	01 1100 1100		01 1100 0011
41	71	D17.3	10 0011 1100		10 0011 0011
40	72	D18.3	01 0011 1100		01 0011 0011
3F	73	D19.3	11 0010 1100		11 0010 0011
3E	74	D20.3	00 1011 1100		00 1011 0011
3D	75	D21.3	10 1010 1100		10 1010 0011
3C	76	D22.3	01 1010 1100		01 1010 0011
3B	79	D25.3	10 0110 1100		10 0110 0011
3A	7A	D26.3	01 0110 1100		01 0110 0011
39	7C	D28.3	00 1110 1100		00 1110 0011
38	80	D0.4	10 0111 0010		01 1000 1101
37	81	D1.4	01 1101 0010		10 0010 1101
36	82	D2.4	10 1101 0010		01 0010 1101
35	84	D4.4	11 0101 0010		00 1010 1101
34	88	D8.4	11 1001 0010		00 0110 1101
33	8F	D15.4	01 0111 0010		10 1000 1101
32	90	D16.4	01 1011 0010		10 0100 1101
31	97	D23.4	11 1010 0010		00 0101 1101
30	98	D24.4	11 0011 0010		00 1100 1101
2F	9B	D27.4	11 0110 0010		00 1001 1101
2E	9D	D29.4	10 1110 0010		01 0001 1101
2D	9E	D30.4	01 1110 0010		10 0001 1101
2C	9F	D31.4	10 1011 0010		01 0100 1101
2B	A3	D3.5		11 0001 1010	
2A	A5	D5.5		10 1001 1010	
29	A6	D6.5		01 1001 1010	
28	A7	D7.5	11 1000 1010		00 0111 1010
27	A9	D9.5		10 0101 1010	
26	AA	D10.5		01 0101 1010	
25	AB	D11.5		11 0100 1010	
24	AC	D12.5		00 1101 1010	
23	AD	D13.5		10 1100 1010	
22	AE	D14.5		01 1100 1010	
21	B1	D17.5		10 0011 1010	
20	B2	D18.5		01 0011 1010	
1F	B3	D19.5		11 0010 1010	
1E	B4	D20.5		00 1011 1010	
1D	B5	D21.5		10 1010 1010	
1C	B6	D22.5		01 1010 1010	
1B	B9	D25.5		10 0110 1010	
1A	BA	D26.5		01 0110 1010	
19	BC	D28.5		00 1110 1010	
18	C3	D3.6		11 0001 0110	
17	C5	D5.6		10 1001 0110	
16	C6	D6.6		01 1001 0110	
15	C7	D7.6	11 1000 0110		00 0111 0110
14	C9	D9.6		10 0101 0110	
13	CA	D10.6		01 0101 0110	
12	CB	D11.6		11 0100 0110	
11	CC	D12.6		00 1101 0110	
10	CD	D13.6		10 1100 0110	
0F	CE	D14.6		01 1100 0110	
0E	D1	D17.6		10 0011 0110	
0D	D2	D18.6		01 0011 0110	
0C	D3	D19.6		11 0010 0110	
0B	D4	D20.6		00 1011 0110	
0A	D5	D21.6		10 1010 0110	
09	D6	D22.6		01 1010 0110	
08	D9	D25.6		10 0110 0110	
07	DA	D26.6		01 0110 0110	
06	DC	D28.6		00 1110 0110	
05	E0	D0.7	10 0111 0001		01 1000 1110
04	E1	D1.7	01 1101 0001		10 0010 1110
03	E2	D2.7	10 1101 0001		01 0010 1110
02	E4	D4.7	11 0101 0001		00 1010 1110
01	E8	D8.7	11 1001 0001		00 0110 1110
00	EF	D15.7	01 0111 0001		10 1000 1110

Appendix D

Gigabit Ethernet Ordered Sets - Partial List

Gigabit Ethernet defines certain combinations of characters called Ordered Sets. The table in this appendix shows a partial list.

Name	Function	Beginning RD	Ordered Set	8 Bit Hex
C1	Configuration - flip disparity	Positive	K28.5 D21.5 config_reg[7:0] config_reg[15:8]	
C2	Configuration - sustain disparity	Negative	K28.5 D2.2 config_reg	
I1	Idle - correct disparity	Positive	K28.5 D5.6	0xBC 0xC5
I2	Idle - preserve disparity	Negative	K28.5 D16.2	0xBC 0x50
R	Carrier extend	Negative Positive	K23.7	0xF7
S	Start of packet	Negative	K27.7	0xFB
T	End of packet	Negative Positive	K29.7	0xFD
V	Error propagation	Negative Positive	K30.7	0xFE

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Numbers

A

B

C

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E

F

November 2015
Version 8.1
English

Viavi Solutions

North America:	**1.844.GO VIAVI / 1.844.468.4284**
Latin America	**+52 55 5543 6644**
EMEA	**+49 7121 862273**
APAC	**+1 512 201 6534**
All Other Regions:	**viavisolutions.com/contacts**
email	**customer.care@viavisolutions.com**